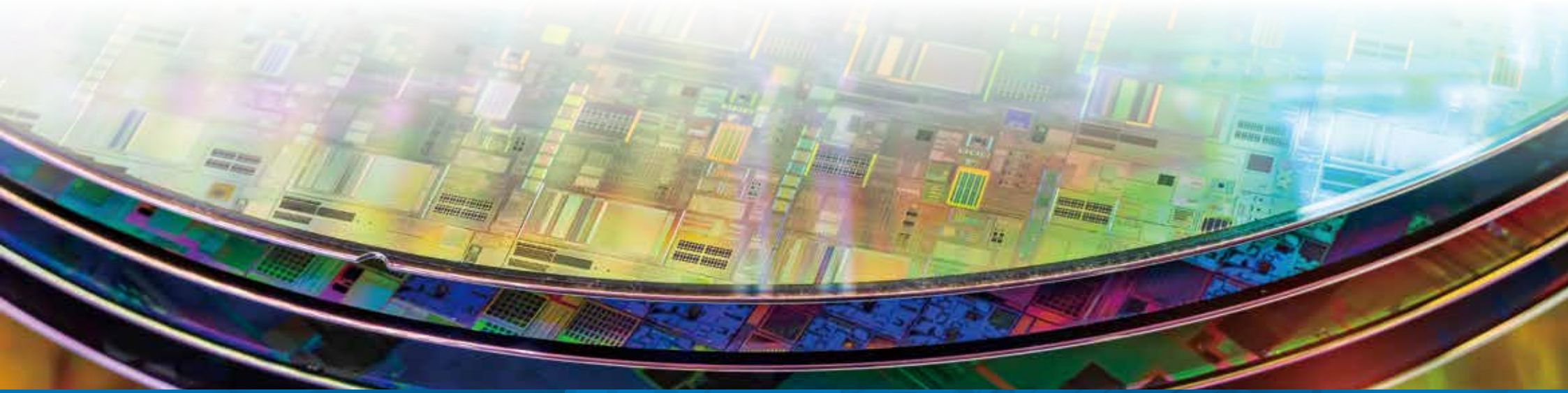
4 Innovative R&D and Green Products

Key Results and Strategies

Strategic Guidelines	Commitment	KPI	2024 Goals and Performance
R&D and Innovation	To become the world-leading provider of customized IC solutions through advanced technologies, seize the key growth opportunities in target markets, focus on sustainability, and collaborate with world-class customers and partners to achieve sustainability goals.	• Increasing the number of patent applications annually.	• The patent allowance rate in various countries is as high as 96% • The number of patents in various countries has reached 154 in the past three years • In 2024, the UCIe 32G IP won the Best IP/Processor of the Year award at EE Awards Asia for its outstanding development technology and specifications
Quality and Customer Relationship Management	Through the PDCA quality management cycle, we ensure the effective implementation of the quality management system, driving continuous improvement in enterprise with the goal of becoming a world-leading IP and ASIC supplier. In terms of customer relationships and communication, we aim to establish seamless partnerships through various two-way communication methods.	• Maintain ISO quality management system certification. • Maintain zero penalty record for regulatory compliance. • Maintaining Customer Satisfaction Above 90%	• Completed ISO 9001 management system re-certification and maintained IECQ QC 080000 and ISO 13485 management system certification. • Received Sony Green Partner certification from the internationally renowned client, becoming a Sony supplier. • In 2024, GUC had neither significant penalty for violations of regulations regarding the provision and use of its products, nor were there any customer complaints or returns due to hazardous substances. • Customer satisfaction rate reached 95% in 2024.

GUC is an upstream provider in the semiconductor industry, specializing in providing comprehensive advanced IC customization services tailored to customer requirements, using Silicon Intellectual Property (IP) to design circuit diagrams for the units, functions, and program codes needed for chips. The Company does not engage in chip production or factory operations. Subsequent manufacturing, packaging, and testing are all conducted by other IC manufacturers.



4.1 Professional IC Design Services and Innovative Technology

GUC provides professional IC design services, with a particular focus on the design of Application-Specific Integrated Circuit (ASIC) products. To meet the requirements of products from concept to finished product with Advanced ASIC Services, GUC collaborates with TSMC to advance high-performance, low-power technologies such as CoWoS, InFO, and 3DIC. The Company also incorporates IP solutions and leverages artificial intelligence in Electronic Design Automation (EDA) to optimize design processes. By partnering with academia, GUC further advances AI technology applications in design services, boosting its market competitiveness. GUC offers optimized solutions for product realization through the following three service models and capabilities:

Non-Recurring Engineering (NRE)	Multiple-Project Wafer (MPW)	Silicon Intellectual Property (IP)
Provides circuit design component libraries and various silicon intellectual properties needed for product design, as well as circuit diagrams for manufacturing product mask sets. The Company then commissions foundries to produce masks, wafers, dicing, and packaging, after which the Company's engineers conduct product testing before delivering prototypes to customers.	Provides a cost-effective and timely chip verification service by integrating designs from different customers, sharing the manufacturing costs of a single mask set and one batch of wafers (Engineer Run). This allows design engineers to achieve low-cost and rapid prototype verification using advanced process technology before mass production.	Designed and verified integrated circuit designs with specific functions that can be reused. With advancements in integrated circuit manufacturing technology, multi-function chips and even SoC have become the mainstream in IC design. Reusable IP can reduce customers' duplicate design efforts and design resource investments.

4.1.1 Providing Advanced ASIC Services

The semiconductor industry supply chain can be divided into four major groups according to upstream, midstream, and downstream: design, manufacturing, packaging, and testing. For the upstream chip design group, the chip design flow goes beyond hardware specification design and also requires software design support. Only after high automation integration can highly efficient, low-power consumption chips be designed at extremely tiny nanometer dimensions. GUC offers upstream IC design services to meet rapidly changing semiconductor industry and diverse customer demands. Our Advanced ASIC Services framework allows customers to enter the semiconductor design industry chain at any stage, from product concept, specification formulation, development, verification, final completion. Specifically, GUC provides advanced special IC design services through the following four core capabilities:

IP Solution	Chip Implementation	ASIC Manufacturing	Advanced Packaging Technology
Help customers reduce design time costs and minimize SoC development risks to meet their customized requirements.	The Company works closely with TSMC, giving a strong command of information on advanced manufacturing processes. This expertise allows us to help customers accelerate their entry into advanced process, achieve faster mass production, improve yield rates, and strengthen market competitiveness.	In addition, GUC actively partners with world-class wafer foundries, packaging and testing companies, and other supporting suppliers to deliver professional, high-quality manufacturing services. This collaboration shortens time-to-market and time-to-volume, lower entry barriers and technical risks, and ensures high quality, high yield rates, and on-time delivery. As a result, customers can focus their valuable resources on their core strengths.	GUC deploys advanced process design platform solutions and advanced packaging technologies, working with TSMC to complete the design and verification of CoWoS, InFO, and 3DIC, meeting the requirements for high performance, low latency, and low power consumption. GUC also continues to develop IPs such as HBM, GLink, and UCIe needed for advanced packaging platforms.

4.1.2 Artificial Intelligence (AI) Technology Applied to IP Design and Design Services

In recent years, the rapid development of Artificial Intelligence (AI) has become an indispensable technological tool for enterprise research and development. When used properly, it can enhance efficiency and reduce waste of resources. GUC IP design team has prioritized the implementation of AI technology for the Monte Carlo simulation, saving computational resources and enabling a 50% reduction in simulation time. This allows limited resources to be reallocated to more design projects.

In addition, GUC has completed the evaluation of AI-based design migration solutions, which help design engineers optimize circuits for enhanced results and reduce the design cycle by 30%. GUC expects to officially implement it by the second quarter of 2025.

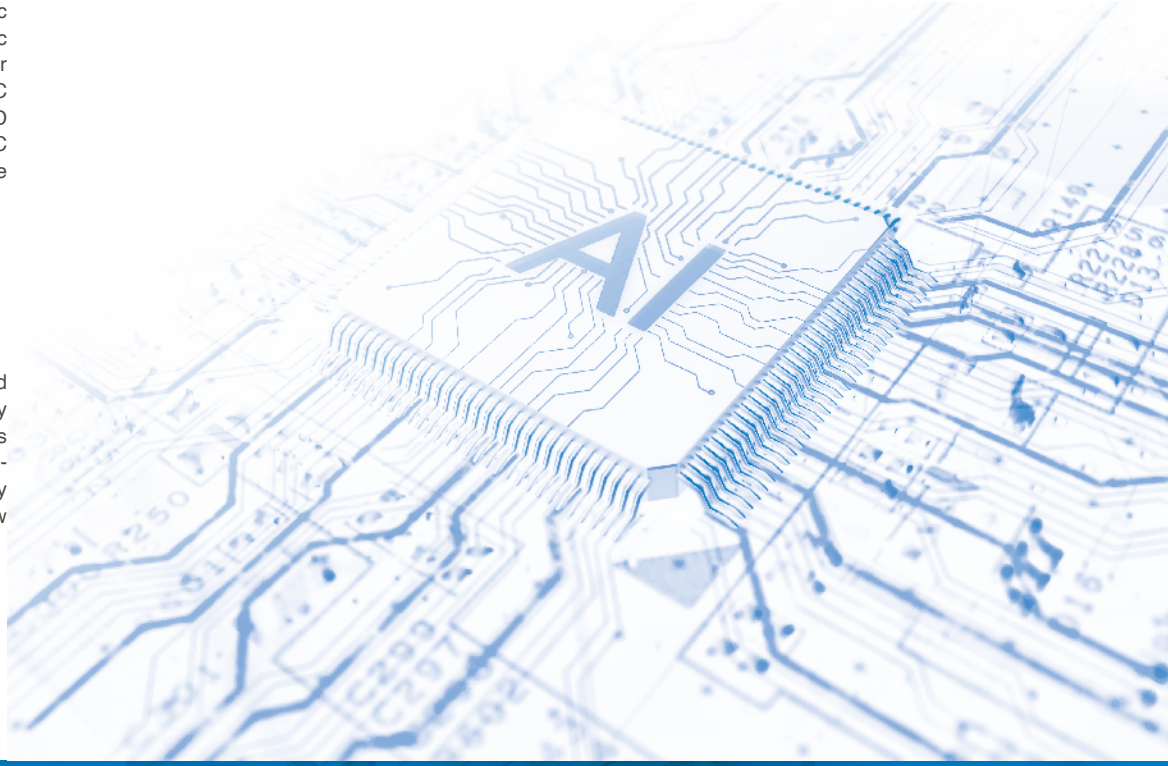
GUC introduced Engineering Change Orders (ECO) tools in 2020, reducing leakage optimization time by 15-30%. In 2023, AI automatic placement and routing technologies and tools were implemented, saving 2-8% in power efficiency. In 2024, GUC collaborated with leading Electronic Design Automation (EDA) companies to introduce AI-driven EDA technologies, applied to automatic floorplan optimization. Preliminary results show a 3% reduction in area while also achieving lower power consumption. In addition to adopting AI-driven technologies from EDA companies, GUC collaborates annually with universities to develop AI and machine learning applications for 2D/3D EDA design flows. These academic partnerships aim to integrate advanced technologies into GUC design service processes, enhancing design quality, efficiency and optimization, and applying the innovations to customer products.

4.1.3 Functional Safety Implementation Technology Applied to Automotive Design Services

Starting in 2024, GUC introduced Function Safety implementation technology and established supporting design implementation service processes, including: (1) System-level logic and memory self-testing, enabling vehicles to self-diagnose critical components. (2) Implementation processes that are USF or SSF Function Safety format aware, supporting dual-core or triple-register decision-making and physical verification to reduce failure rates. These technologies enhance the safety of customers' automotive products. We will continue to monitor industry trends and develop new technologies to make future automotive solutions even safer and more user-friendly.

4.2 Innovative R&D and Quality Management

GUC's adoption of CoWoS and InFO chiplet architecture has become mainstream for infrastructure products. Backed by close collaboration with key partners, GUC's R&D team brings years of experience in High Bandwidth Memory (HBM) and GUC multi-die interLink (GLink) IP development, as well as in the mass production of CoWoS products. To help customers stay competitive in the 2.5D/3D advanced packaging domain and maintain their market leadership, GUC remains committed to delivering industry-leading comprehensive 2.5D solutions, including the industry's first silicon-validated HBM3 physical layer and controller, GLink 2.5D and 3D chiplet interfaces, electrical and thermal simulation, package design, DFT and production testing, and CoWoS and InFO manufacturing expertise.



4.2.1 Successful Technology Development and Innovation Achievements in 2024

In addition to developing advanced process (5/4/3/2 nm, etc.) silicon intellectual property— including ultra-high-speed interface chip interconnect IP like, UCIe, GLink-2.5D/3D, HBM2/2E/3/3E/4 Controller and PHY components, as well as high-speed ADC/DAC—GUC also migrates existing key fundamental components, such as Power Management Solutions and Clock Generators, to more advanced processes. GUC has also established a dedicated R&D team focused on developing proprietary memory IP (such as TCAM, SRAM), customized standard cells, and an extensive database of proprietary IP and libraries, offering customers more comprehensive solutions.

To support future growth, GUC will continue investing in R&D resources to optimize 5/4/3/2 nm design flows, while advancing the development of ultra-high-speed interface chip interconnect IP, including GUCIe, GLink, GLink3D, HBM PHY & Controller, High-speed ADC, TCAM, and so on.

GUC Innovation Achievements Overview for 2024

First Quarter	• By leveraging TSMC InFO/CoWoS packaging technology, the third-generation 5nm chip interconnect IP, GLink2.3, was successfully migrated to 3nm, providing customers with comprehensive multi-chip interconnect solutions • The design of a 6nm high-performance computing chip has been finalized, with mass production in 2024 • As a leading company, GUC also completed silicon validation in 2024 for its HBM3E (PHY & Controller) IP with DRAM manufacturers' 12Hi HBM3 and HBM3E • The 3nm UCIe/32G chip interconnect IP completed its design finalization in November 2023, and is expected to complete silicon validation in the first quarter of 2025, offering customers comprehensive multi-chip interconnect solutions compliant with UCIe interoperability standards • Leveraging TSMC's advanced process, integrating AI/HPC chips designed by customers for large-scale cloud data centers with 2.5D CoWoS packaging technology, GUC has successively enabled multiple customers to achieve mass production. Notably, in 2024, 5nm AI customers adopting HBM3E memory entered mass production • The 3nm HBM3E 9.4G (PHY & Controller) IP design has been finalized, supporting both TSMC's CoWoS-S and CoWoS-R packaging technologies. Meanwhile, the silicon validation was completed in the first quarter of 2024, and the IP has already been adopted by multiple customers • Leveraging TSMC's 3DFabric chip stacking technology, GUC has launched 6nm and 5nm GLink-3D chip interconnect IPs, both of which have completed silicon validation
Second Quarter	• Completed the development of the design flow for the 3nm enhanced version.
Third Quarter	• The 5nm long-distance optical communication chip design was finalized and taped out in the third quarter of 2024 • The 3nm long-distance optical communication chip design has been started, will be taped-out in the fourth quarter of 2025.
Fourth Quarter	• The 2nm mixed-signal PLL, THM, and Process Monitor IP design has been finalized, with silicon validation scheduled for completion in the second quarter of 2025 • The 2nm design flow and optimized cell library has been completed and successfully applied to 2nm testchip project • Adopted TSMC's System on Wafer (SoW) technology to support customers in completing the design and tape out of mechanical test vehicle • The 5nm Edge Computing-grade Artificial Intelligence chip (Edge AI) and the advanced version of the 16nm Virtual Reality chip (Metaverse) have completed Spec-in design finalization

4.2.2 Green Product Quality and Competitiveness

In a highly competitive market, GUC encourages all employees to provide customers with high quality design services, silicon intellectual property, and competitive products in the spirit of innovation and continuous improvement, and is committed to listening to our customers. GUC is dedicated to listening to customer feedback and building trustworthy, mutually beneficial partnerships with customers. Through the PDCA quality management cycle, we ensure the effective implementation of the quality management system, driving continuous improvement in enterprise with the goal of becoming a world-leading IP and ASIC supplier.

GUC is committed to delivering exceptional ASIC IC design services. The Company's Quality and Reliability organization continuously refines the ISO quality management system, maintaining its ISO9001 certification annually. By identifying opportunities for improvement in total quality management, GUC ensures complete customer satisfaction, with recertification completed in 2024. In addition, we have obtained Sony Green product certification from the internationally renowned customer Sony, becoming a Sony supplier. In February 2025, we were recognized by international brand SK hynix Green Partner certification for compliance with RoHS Directive and customer's requirements.

GUC is deeply committed to green products, starting with Eco-design solution. Through continuous technological innovation, we meet with customers' special requirements for hazardous substances, consistently working to reduce and regulate banned substances. We maintain the IECQ QC 080000 management system certification annually, with third-party verification to ensure the effectiveness of our green product management. Our unremitting efforts have been recognized and certified, with the latest certification valid until August 2025. GUC's green ICs comply with the EU RoHS Directive and the EU Registration, Evaluation, Authorization and Restriction of Chemicals (EU REACH) regulations, ensuring the non-use of restricted. Based on customer-specific requirements, GUC was commissioned by customers in 2024 to conduct compliance investigations, including: IPC1752, chemSHERPA material declaration statements and other international regulations, and provided the investigation results to customers. Furthermore, to ensure that the production process of green ICs complies with regulatory requirements, we conduct quarterly business review (QBR) with designated suppliers, including HSF (hazardous substances free) compliance item and regularly evaluate the execution results each quarter.

GUC QualityManagement System Certifications Overview

GUC ISO9001 Certification

GUC IECQ QC080000 Certification

Sony Green Partner certification

GUC ISO 13485 Medical Certification

SK hynix Green Partner Certification

4.2.3 Customer Service and Satisfaction

In addition to maintaining management system certifications, GUC ensures the delivery of high-quality IC design services. We also strengthen customer relationship management through regular and irregular meetings and visits, as well as quarterly and monthly performance reviews or audits. These efforts help build seamless partnerships and align both parties with short, medium, and long-term development goals and social responsibility initiatives. To provide localized customer service, we have established dedicated offices in six regions—Taiwan (headquarters), China, Japan, Korea, the United States, and Europe—with dedicated service contacts. These contacts support the planning and implementation of environmental management, social responsibility, hazardous substance control, and conflict minerals between both parties, while complying with ISO9001 and accepting third-party verification. We promptly provide sufficient information to meet the needs of downstream and end customers, or public sectors, and actively cooperate with customers' corporate social responsibility programs to implement activities, investigations, audits, and data collection.

To ensure customer satisfaction with GUC's service quality, we conduct customer satisfaction surveys annually in the first quarter or upon project completion. Customers are invited to provide feedback on GUC's service quality and effectiveness through ratings, comments, or comparisons with competitors. A dedicated customer satisfaction team follows up with concrete responses, tracks improvement progress across responsible departments, and performs detailed data analysis to identify root issues. These results are compiled into reports for senior management as reference for medium and long-term operational planning.

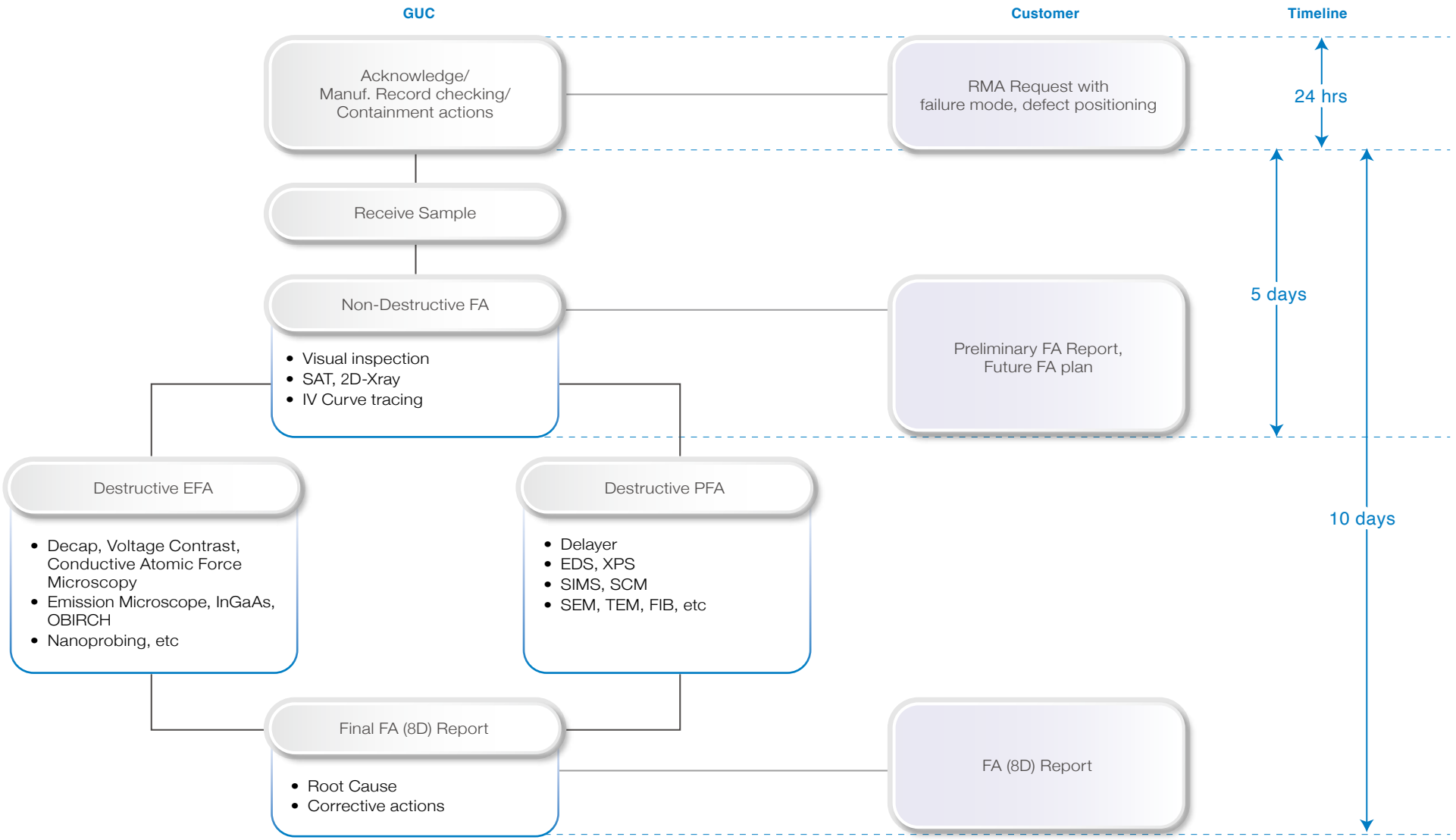
Statistics of Customer Satisfaction Survey

Year	Customer Average Satisfaction
2022	95%
2023	97%
2024	95%

As of 2024, the customer satisfaction surveys over the past five years have consistently achieved a response rate of over 80%, with more than 90% of respondents rating their satisfaction with GUC as "Satisfied" or higher. This reflects GUC's ability to continuously enhance service effectiveness and maintain high customer satisfaction amid technological advancements and a highly competitive business environment. In the 2024 customer satisfaction survey, most customers gave highly positive feedback, praising GUC for its quick response, rigorous and reliable design process, proactive approach to problems, robust supply chain protection, stable quality and guaranteed production capacity, professional technical team, and reliable technology and service, giving GUC the highest affirmation.

Regarding customer complaints, we have established a Customer Complaint Management Procedure, requiring relevant departments to respond to customers within 24 hours of receiving a complaint and provide a preliminary analysis report within five working days. In 2024, the on-time response rate for preliminary analysis reports of customer complaints reached 90%.

GUC Customer Complaint Handling Process



4.2.4 Green Product Sustainable Management and Practices

GUC implements a PDCA management process for green product sustainable management to address regulatory risks. Improvement strategies are proposed through supplier surveys, and we work closely with the supply chain to prevent the use of hazardous substances. These efforts aim to proactively respond to international regulatory trends and enhance the competitiveness of GUC products. To ensure green IC production process complies with regulatory requirements, we conduct the Quarterly Business Review (QBR) procedures for seven designated suppliers and evaluate the implementation results on a quarterly basis. In 2024, all GUC products met customer and regulatory requirements without any compliance violations, and all design materials adhere to the special requirements for customers' green products.

- Management Review: The top management review the achievement of hazardous substance KPIs.
- Customer Satisfaction: Annual customer satisfaction surveys regarding green product management are conducted to review customer feedback.

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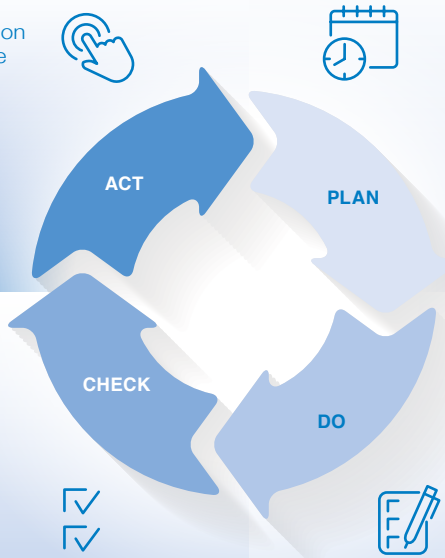
- Achieve 89% customer satisfaction rating high ratings and positive recognition for green product sustainable management. We are recognized by customer SK hynix to obtain Green Partner Certification in Feb'25



- Regulatory identification and customer requirements
- Restricted substance regulations
- Planning for hazardous substance substitution

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- The European Union has added seven new substances to the Registration, Evaluation, Authorization and Restriction of Chemicals (REACH) regulation. In 2024, the EU candidate list has been expanded to 242 SVHCs. GUC complied with all new requirements. We continuously monitor updates to the REACH regulations and have obtained supplier compliance declarations that are 100% compliant with the new requirements.
- Investigating whether the supply chain uses per- and polyfluoroalkyl substances (PFAS compounds) and continuously monitoring regulatory developments.

- Raw material hazardous substance test
- Suppliers are required to provide the proof of compliance with hazardous substance test report issued by ISO 17025 certified labs.

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- Require suppliers to provide third-party test reports to ensure the compliance of raw material and meet with GUC specification.

- Evaluate and Review Material from product Eco-Design Stage
- Implement elimination of Hazardous substance program

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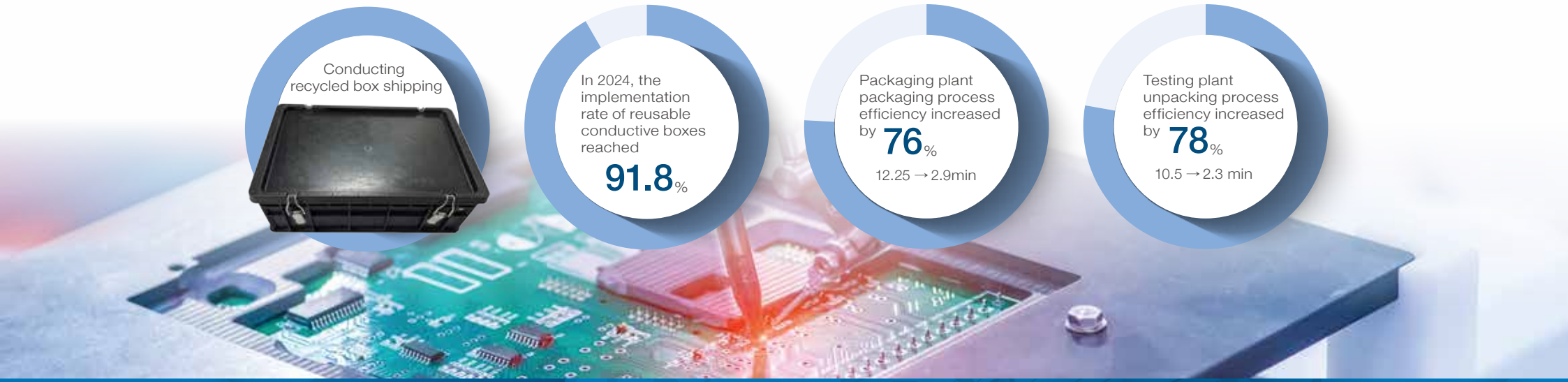
- In the Bill of Materials (BOM) material selection phase, 18 new product BOMs were added in 2024, adopting green IC specifications.
- GUC investigation planned to identify emerging chemical risks and assess the use of Per- and Polyfluoroalkyl Substances (PFAS). The European Chemicals Agency ("ECHA") has unveiled a proposal that would ban the production, use, and sale of about 10,000 per-and poly-fluoroalkyl substances ("PFAS")* in the European Union. The proposal is in the evaluation stage with ECHA's final proposal. Perfluorinated and polyfluorinated alkyl substances (PFAS) are known as 'forever chemicals' as they are extremely persistent in our environment and bodies. They can lead to health problems such as liver damage, thyroid disease, obesity, fertility issues and cancer. PFAS are of concern because of their high persistence (or that of their degradation products) and the impacts on human and environmental health. GUC is committed to actively reduce hazardous substances starting from the product design phase. We would follow aforementioned proposal whenever it announce. We have evaluated new standard early and completed the screening of 93 products to ensure that we use safer materials and comply with environmental standards. Now we continue to update the review and assess all potential hazardous substances that may impact environment with our suppliers to research safer substitutes. GUC strives to do proactive elimination of Hazardous substance from the product design stage.

4.2.5 Hazardous Substance Sustainable Management and Actions Throughout Product Life Cycle

Measures	Green IC Design and Requirements	Green Material Selection	Green IC Manufacturing	Green Packaging Use
Description	GUC responds to customer requirements for green materials by adhering to green procurement procedures and selecting materials that comply with international regulations, including RoHS, EU chemical policy (REACH), with the EU candidate list increased to 242 substances in 2024, and continues to monitor updates to the REACH regulated substance list. As well as Ozone Depleting Substances (ODS), and Persistent, Bioaccumulative and Toxic (PBT) substances under the US TSCA. To ensure environmental protection, all products use halogen-free materials, and we actively seek alternative materials to avoid the use of harmful substances in raw materials.	In the Bill of Materials (BOM) material selection stage, GUC actively conducts risk assessments, with 18 new product BOMs added in 2024, adopting green IC specifications. At the same time, GUC sets strict restrictions on product materials to eliminate harmful substances, aiming to prevent any part of the production processes from potentially impacting the environment, such as contributing to global warming and ozone layer depletion.	GUC has strengthened its hazardous substance management mechanism by requiring suppliers to monitor hazardous substances in raw materials and to provide third-party test reports to ensure compliance with green product principles and international regulations. In 2024, all customer-commissioned investigations were able to provide customers with compliance investigation results.	Product packaging materials are restricted according to the Packaging Directive (94/62/EC). The following are GUC's concrete actions to comply with international regulations and promote circular economy: • Green IC production requirements for restricting hazardous substances in product packaging: In 2023, the France Decree 2020-105 was added, which regulates mineral oil substances in ink packaging. Mineral oil saturated hydrocarbons (MOSH) and mineral oil aromatic hydrocarbons (MOAH) have been proven to be carcinogenic and bioaccumulative. To comply with international regulatory trends and protect customer health, we strictly inventory and control the compliance level of 14 suppliers. In 2024, after GUC's guidance, suppliers are 100% compliant with requirements. • Introduction of reusable conductive boxes: Considering the environmental impact of discarded packaging materials, GUC has adopted reusable conductive boxes to replace single-use cardboard boxes, implementing waste reduction (Reduce), recycling conductive boxes back to the factory for reuse (Reuse), and recycling (Recycle), aiming to minimize environmental impact. Additionally, GUC has simplified the packaging process for products transported from the packaging plant to the testing plant. This includes streamlining packaging and unpacking processes, such as eliminating inner packaging steps for large boxes, which also reduces operational time waste. In 2024, the implementation rate of reusable conductive boxes reached 91.8%.



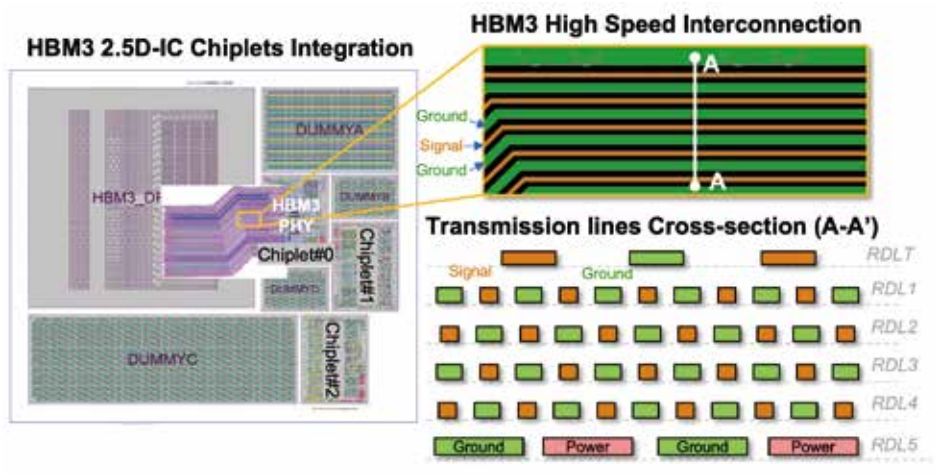
4.2.6 HBM3E CoWoS Advanced Packaging Eco-Design Solution

GUC's Eco-Design adopts the HBM3E CoWoS advanced packaging eco-friendly solution, incorporating environmental considerations at the product packaging circuit design stage. Featuring high speed and low power consumption, it minimizes environmental impact from the design source, reducing energy consumption while maintaining superior signal quality. It is applied in areas such as artificial intelligence and servers. In terms of environmental benefits, compared to the original circuit design method that caused 36.58 kg CO2e/year in greenhouse gas emissions, the environmentally friendly IC design solution produces 33.91 kg CO2e/year in emissions, achieving an energy saving benefit of 7.3% reduction.

Greenhouse Gas Reduction Performance Chart of New CoWoS Technology

To meet the goals of HBM3 high-speed transmission and low power consumption, this design proposes a high-speed signal transmission architecture (GSG interleaved transmission line), applied to advanced packaging processes for HBM3 chip-to-chip high-speed interconnection configurations. This has been successfully applied in the verification of two chip designs, including TSMC's 7nm and 3nm processes, along with corresponding advanced packaging verification chips.

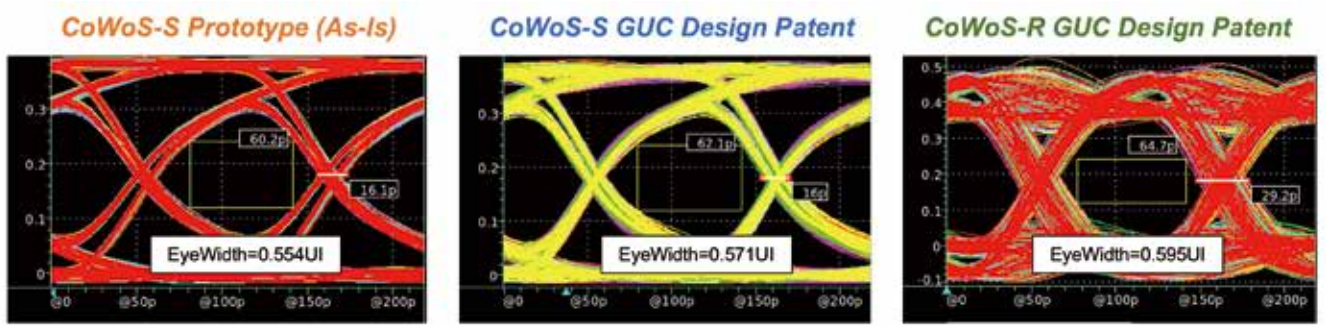
High-Speed Signal Transmission Architecture Demonstration

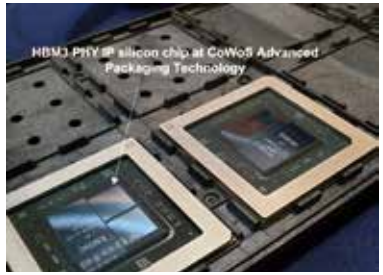


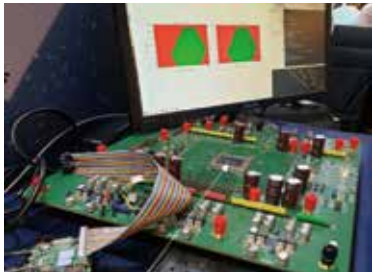
In the high-speed transmission advanced packaging process, through the circuit design architecture (design patent) proposed by this design, circuit load can be effectively reduced, thereby enhancing signal transmission quality, with transmission speed increasing up to 9.2 Gbps. In the analysis, the original design's circuit load in the silicon interposer process (CoWoS-S) is 1.92 pF, with a power consumption of 8435.2mW, and a signal eye width of 0.554 UI. By adopting this design's circuit architecture, the silicon interposer process achieved a reduced circuit load of 1.49 pF, with power consumption of 8194.4mW, and an improved eye width to 0.571 UI. When applied to the organic material interposer process (CoWoS-R), the circuit load can be further reduced to 0.85 pF, power consumption lowered to 7836mW, and eye width increased to 0.595 UI. Both the silicon interposer and organic material interposer process can leverage this circuit architecture to meet high-speed interconnection transmission requirements, offering low loss, low crosstalk, and optimized signal quality.

	Original Design of Silicon Interposer Process CoWoS-S Prototype (AS-is)	Silicon Interposer Process with Circuit Design Design Patent@CoWoS-S (To-Be)	Organic Material Interposer Process Design Patent@CoWoS-R (This-Work)
Parasitic Capacitance	1.92pF	1.49pF	0.85pF
Power Energy Efficiency (pJ/bit)	0.9	0.87	0.83
Eye Width (UI)	0.544	0.571	0.595
Power Consumption (mW)	8435.2	8194.4	7836
Greenhouse Gas Emissions ($kgCO_2e$)	36.58	35.46	33.91
Energy Saving	-	3.10%	7.30%

- **Signal eye diagrams of high-speed transmission for the three main advanced packaging processes mentioned above.**







4.3 Patents and Silicon Intellectual Property

GUC offers comprehensive ASIC (Application-Specific Integrated Circuit) design services, offering design and mass production services for customers' end-application products. Our ASIC design services include SoC development and verification, advanced design flow, low-power solutions, advanced design for testability, and flagship chip design solutions. For ASIC production services, we provide advanced packaging technology, testing, product engineering, quality and reliability, and supply chain management services. Furthermore, GUC possesses the capability to develop its own Silicon Intellectual Property (IP), positioning itself as an IP supplier. To this end, we are dedicated to innovative research and development of various competitive Silicon Intellectual Property (IP), including High Bandwidth Memory (HBM) IP, Chip Interconnect (GLink-2.5D/3D) IP, Mixed-Signal Front-End IP, and Embedded Memory IP.

Number of Granted Patents by Country

Country	Number of Patents
Taiwan	219
United States	208
China	117
Japan	16

To safeguard the outcomes of innovative research and development, GUC files patent applications for competitive technical solutions generated throughout the ASIC design and production service stages. In parallel, we implement patent strategies for our proprietary Silicon Intellectual Property (IP). By securing patent protection, GUC not only maximizes the benefits and competitive edge of its R&D achievements but also offers customers enhanced protection for their ASIC products. Recognizing the importance of patent rights, GUC has been offering engineers with intellectual property-related in-person courses annually since 2016. These courses aim to strengthen awareness of patent rights and promote momentum for patent proposals. Since its establishment, GUC has obtained 560 patents from various countries. In recent years, the company has been actively deploying patents related to CoWoS, HBM, G-Link, and other technologies to maintain its leading position and competitive advantage.

Intellectual Property Rights Management

To foster innovation, maintain a competitive edge, and protect research and development outcomes, GUC established the Intellectual Property Management Regulations in 2016. Since 2000, the Company has been promoting intellectual property rights management plans and has formulated the Patent Proposal Application Procedure as a guideline for patent application, maintenance, utilization, and bonuses/rewards related matters. To carefully evaluate patent proposals, the Company has further established an internal patent review mechanism called the Patent Committee. Committee members include senior executives from relevant departments and heavyweight professors specially appointed from the IC design field externally. Through the committee's internal review and opinions, the technical content of invention proposals can be made more complete, effectively ensuring patent quality and increasing the probability of patent approval. In the past three years, the Company has filed a total of 167 patent applications in various countries, with 55 cases completing the examination process. Among these, 53 were granted and two were abandoned, while the rest are still under examination. This demonstrates that our company's patent allowance rate across various countries is as high as 96% (53/55=96%). In addition, for patent proposals that are unsuitable for public disclosure but have technical value, the Patent Committee may decide to protect them as trade secrets instead, preventing the leakage of confidential technologies.

In addition, to effectively enhance management efficiency, GUC introduced the Patent Management Information System in 2015 as an information management platform for patent proposals, applications, maintenance, bonus distribution, technology classification, and product applications. With the support of this information system, GUC enhances the protection of confidential patent information, while also improving staff efficiency and reducing human errors in the patent application processes.

Additionally, GUC regularly conducts patent inventory operations to review the application status of patents and their degree of relevance to related products, providing an evaluation of patent value. To further strengthen awareness and respect for patent rights among R&D personnel, and to prevent violations of patent boundaries, the Company requires all new R&D personnel to complete basic patent courses. In addition to these fundamental courses, the Company regularly invites patent industry instructors to offer intellectual property-related practical courses for our R&D team, including patent search, infringement identification, design-around, and other advanced courses. As of 2024, a total of 235 employees have participated in these courses.

To maintain a leading position in industry technology, GUC adopts a strategy that integrates key operational development objectives with intellectual property rights protection. For specially developed Silicon Intellectual Property (IP) and Advanced Packaging Technology (APT)—such as CoWoS, HBM, and G-Link—patent engineers collaborate with relevant R&D personnel to review the research, development, design processes, and outcomes to evaluate the feasibility of patent applications. For projects with patent layout potential, GUC actively files patent applications and continuously tracks the proposal progress. By progressively implementing patent layout for specifically developed Silicon Intellectual Property (IP), GUC not only strengthens its competitive edge in specific fields but also implements the Silicon Intellectual Property (IP) Project/IC Product Patentization to fulfill the goal of securing patent protection for key Silicon Intellectual Property and IC product developments. Meanwhile, the Company conducts regular patent technology inventories as a basis for managing the correlation between patent intellectual property and Silicon Intellectual Property (IP), as well as for evaluating the value of patent intellectual property.

To ensure that senior management fully understands the implementation of our intellectual property management plan, the legal supervisor reports on this matter to the Board of Directors at least once a year.

4.4 Green Product Design Services

During the chip tape out process, GUC generates power consumption data and provides power consumption models to enable design engineers to optimize power efficiency throughout the chip design cycle, effectively managing the overall energy consumption of the chip. Moreover, GUC is committed to delivering comprehensive power solutions for customers in the area of packaging design.

Silicon Intellectual Property (IP) In addition to developing advanced process technologies such as 5/4/3/2 nm Silicon Intellectual Property (SIP), including ultra-high-speed interface chip interconnect IPs like GUCIe, GLink, GLink3D, HBM2E/3 Controller and PHY, and high-speed ADC/DAC, GUC is also migrating key fundamental components, such as Power Management Solutions and Clock Generators, to more advanced process technologies.	High Bandwidth Memory IP (HBM3 IP) GUC's latest 8.6G High Bandwidth Memory (HBM3) IP completed silicon validation in the second quarter of 2024 and has already been adopted by multiple customers. Compared to the previous generation, the new 3nm products deliver an approximate 11.3% reduction in power consumption, enabling customers to develop products that balance high performance with energy efficiency. GUC's HBM3 IP, with its excellent development technology and specifications, was awarded Best IP of the Year at EE Awards Asia in 2023.
	Ultra-high-speed Interface Chip Interconnect IP (GLink 2.5D) Since 2020, GUC has leveraged TSMC's InFO packaging technology to launch the high-performance GLink series chip interconnect IP, continuously enhancing product performance and energy efficiency. In 2023, GLink 2.3 IP completed its 3nm process design finalization and was validated in 2024. Compared to similar industry products with UCIe IP specifications, the new GLink 2.3 IP product significantly reduces power consumption by 28%, effectively decreasing energy consumption in customer products, and demonstrating its leading technological position.
	Universal Chiplet Interconnect Express IP (UCIe) In early 2022, GUC released UCIe 1.0, aiming to standardize packaging and advanced packaging die-to-die interfaces, thereby fostering ecosystem collaboration for multi-chiplet integration. GUC continues to leverage its GLink-2.5D experience and expertise to develop the next-generation GUCIe, featuring the highest specification UCIe (32Gbps per channel). The 3nm product was finalized in the fourth quarter of 2023, with the validation report expected to be completed by the first quarter of 2025. The 5nm low-power product is scheduled to finalize its design in the fourth quarter of 2024, featuring an increased speed of 40Gbps, and the validation report is expected to be completed by the fourth quarter of 2025. Compared to GLink-2.5D, the UCIe 32G IP is expected to significantly improve beachfront efficiency (data transmission efficiency per unit area width) by more than 100%. Recognized for its outstanding development technology and specifications, the UCIe 32G IP was named Best IP/Processor of the Year at the 2024 EE Awards Asia, further strengthening GUC's technological strength and innovative capabilities.
	GLink-3D Chip Stacking Interface IP 3D packaging is an advanced technology that increases transistor density. As an industry leader, GUC has partnered with TSMC to develop the GLink-3D 1.0 product, enabling 3D SoIC stacking for 5nm and 6nm chips. The validation report was completed in 2024. The next-generation GLink-3D 2.0 will feature enhanced product specifications and is expected to finalize its design by mid-2025. The new version will support 5nm and 3nm chip stacking with a smaller bond pitch, increasing signal bandwidth density by approximately three times, aiming to significantly reduce power consumption by 80%

System-on-Chip (SoC)

As technology advances into the era of internet, wireless communications, smartphones, IoT, automotive electronics, and AI high-performance computing, system-on-chip (SoC) that integrates more functions has become the mainstream in integrated circuit (IC) design. However, high integration presents complex design challenges, and issues such as design timelines, costs, and specification constraints, arising from advanced manufacturing processes, are unavoidable. To help customers achieve their market goals, the SoCRD department continuously works to enhance design integration and verification technologies, aiming to shorten project timelines and deliver optimal solutions for power consumption, performance, and cost.

System-on-Chip/Silicon Intellectual Property Automatic Integration Process (SoC/IP Constructor, unicoRn)

Since 2021, GUC's SoCRD department has successfully completed a range of chip designs, including 16nm autonomous driving chips (Automotive), 12nm 5G networking chips (Networking). In 2022, the team completed 7nm virtual reality chips (Metaverse). In 2023, the department completed 5nm data center-grade AI chips (Datacenter AI) and production version of 16nm automotive chips. In 2024, the SOC department finalized 5nm edge AI chips and the advanced version of 16nm virtual reality chips.

- Over the years, GUC's SoCRD department has relied on:
  1. Enhanced R&D capacity and industry-leading integration verification processes, effectively reducing pre-production timelines by 30~50%.
  2. Early identification of critical debugging items during integration, saving 30~50% of resources that would otherwise be used for extensive functional simulation and late-stage regression debugging.
  3. Optimization of chip specifications based on manufacturing process advancements, improving performance by 20~30%, reducing power consumption by 15~20%, and decreasing chip area by 20~30%.
- The System-on-Chip/Silicon Intellectual Property automatic integration process is as follows:
  Step 1. Critical subsystem (processor, high-speed interface, memory) integration platform (Subsystem)
  Step 2. Hardware accelerator-based advanced verification process (Emulation)
  Step 3. Low-power design verification and optimization (Power profiling)
  Step 4. Software and hardware co-verification process (Virtual/Hybrid platform)

Design Services

GUC continuously refines its advanced design technology processes and successfully completed the N3P1.0 and N2v0.9 design flows in 2024, enabling customers to adopt more advanced and efficient manufacturing processes. Through improvements in EDA software and design flows under the consistent design verification, the overall design flow achieves better power consumption and performance. Compared to N3E, N2v0.9, it further reduces power consumption, delivering energy savings by 23.08%. GUC will continue developing N2P and future A16 nanometer design flows to support IP designs with lower-power manufacturing processes, enhance competitiveness, apply them to customer projects, and accelerate customers' progress toward greener products.

Process Comparison: Power comparison between N3Ev1.1 and N2v0.9

Process - Components	N3E v110 – M143	N3P V100 – M143	N2 H130, v0.9
Power (uW/MHz)	10.40	9.60	8.00
Power reduction rate (compared to N3E-M143)	-	7.69%	23.08%