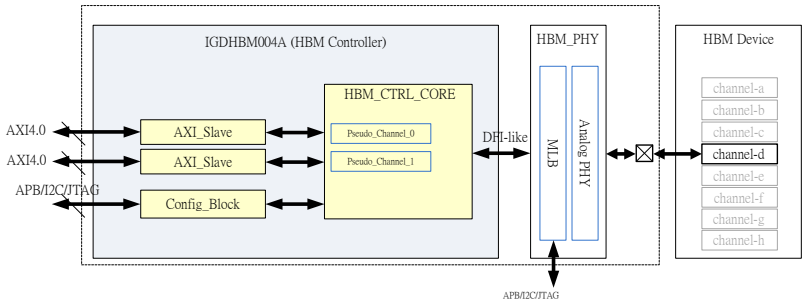
IGDHBM004A
HBM Controller

Overview

IGDHBM004A is a High Bandwidth Memory (HBM) DRAM controller IP, which complies with JEDEC HBM3 Draft Specification Rev. 1.1. Three interfaces are provided to interface with the system bus, HBM PHY, and configuration interface. AXI is the default system bus interface. DFI is the interface between the HBM controller and PHY. Configuration interface can be APB/AHB, I^2C, and JTAG. Users could program IGDHBM004A configuration registers through these interfaces.



Block Diagram

Features

- High Bandwidth Memory (HBM) DRAM controller
- Supports AXI 4.0 port
- Supports DFI1: 2
- Supports BL8
- Supports AWORD/DWORD bus parity check
- Supports ECC & SEV
- Supports synchronous & asynchronous mode
- Supports pseudo channel mode; 32DQ per pseudo channel
- Supports configurable AXI Command/Data FIFO depths
- Supports AXI read interleaving
- Support programmable bit mapping
- Supports DBIac
- Supports manual self-refresh and auto self-refresh
- Supports BIST
- Support single bank Refresh
- Support up to 8.4 Gbps
- Support up to 32Gb per channel
- Support high-performance scheduling and QoS

Applications

- Artificial Intelligence
- Machine Learning
- High-Performance Computing

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Digital Database	.gz

Note: the digital database contains RTL source code, synthesis constraint files, and simulation test bench

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GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

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