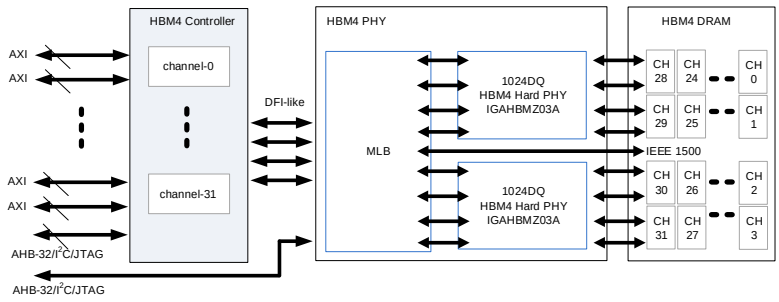
IGAHBMZ03A
TSMC CLN3FFP
HBM4 PHY

Overview

IGAHBMZ03A is a High Bandwidth Memory 4 Physical Layer (HBM4 PHY) that is compliant with JEDEC HBM4 DRAM Specification JESD270-4. Fabricated in the TSMC 3 nm Advanced process node (N3P), it supports the data rate up to 12 Gbps per data pin in the DDR PHY Interface (DFI)-like 1:4 clock frequency ratio (HBM4 controller clock: WDQS = 1:4). The signal and power integrity is analyzed by the GUC design flow to meet all signal and power requirements.

GUC HBM4 PHY includes a hard PHY and a Register Transfer Level (RTL) soft module. The hard PHY, IGAHBMZ03A, includes Command Address (CA) modules, data modules, IO pads, a Phase-Locked Loop (PLL), and Delay-Locked Loops (DLLs). The RTL soft module, also called Miscellaneous Logic Block (MLB), is included to work with the hard PHY for functions, such as the training logic, the register controller interface, the Built-In Self-Test (BIST) logic, and the IEEE 1500 function logic.



Block Diagram

Features

- HBM4 data rate: up to 12 Gbps
- DFI-like 1:4 clock frequency ratio (HBM4 controller clock: WDQS = 1:4)
- Only Burst Length 8
- AWORD/DWORD bus parity
- Programmable parity latency
- HBM4 Data Bus Inversion (DBI)
- 64DQ ECC/SEV per channel
- HBM4 Hard PHY delivered as a hard macro including IO, PLL, and DLL
- Internal Loopback and WRITE/READ BIST
- HBM4 loopback test, including MISR and LFSR modes
- IEEE 1500 Instruction
- HBM4 lane repairs with redundant pins for row/column/data
- HBM4 Duty Cycle Adjuster (DCA) and Duty Cycle Monitor (DCM) training.
- HBM4 AWORD write eye/VREF/perbit training
- HBM4 WDQSK2CK training
- HBM4 DWORD write/read eye/VREF/perbit training
- Broken lane detect and repair
- DLL compensation to overcome VT variation
- HBM4 DWORD write eye retrain to overcome Device VT variation

Technology

- Process: TSMC 3 nm 0.75 V/1.2 V CMOS LOGIC FinFET Advanced Process
- Special layer & device: SVT, LVT, LVTLL, ULVT, ULVTLL and ELVT
- Metal scheme: 1P17M (1Xa_h_1Xb_v_1Xc_h_1Xd_v_1Ya_h_1Yb_v_4Y_hvhv_4Yy2Z)

Applications

- For applications with high performance & high bandwidth memory, such as AI/ HPC.

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4.	Testing Guide	.pdf
5.	PKG & PCB Guide	.pdf
6	Verilog Model	.v
7	Timing Model (LIB/DB)	.lib/.db
8	LEF Model	.lef
9	DRC/LVS/ANT/ERC/CNOD Report	.rep
10	Netlist (Protected)	.spi
11	GDSII (Protected)	.gds

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC IP Eco-System provides the flexibility to work with IP from GUC, TSMC, and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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