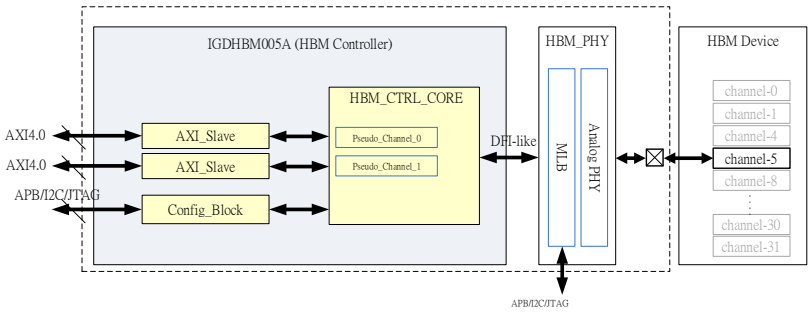
IGDHBM005A
HBM Controller

Overview

IGDHBM005A is a High Bandwidth Memory DRAM (HBM4) controller IP, which complies with JEDEC HBM4 Draft Specification Rev. 0.91. Three interfaces are provided to interface with the system bus, HBM PHY, and configuration interface. AXI is the default system bus interface. DFI is the interface between the HBM controller and PHY. Configuration interfaces can be APB/AHB, I^2C, and JTAG. Users could program IGDHBM005A configuration registers through these interfaces.

IGDHBM005A supports flexible AXI addressing mapping, suitable for different AXI Master transaction scenarios. The read-after-write forwarding scheme eliminates the collision between reading and writing. The IGDHBM005A also supports auto clock gating and auto power down mode, which can decrease power consumption. The IGDHBM005A also supports SEV and ECC write-back features to protect the data correcting when the SEV or ECC error happens.



Block Diagram

Features

- High Bandwidth Memory DRAM (HBM4) controller
- Supports AXI 4.0 port
- Supports AWORD/DWORD bus parity check
- Supports ECC & SEV and Write Back
- Supports pseudo channel mode; 32DQ per pseudo channel
- Support DBIac
- Supports configurable Command/Data FIFO depths
- Supports AXI configurable AXI address mapping
- Support Read-After-Write
- Support AXI read interleaving
- Supports manual self-refresh and auto self-refresh
- Supports manual power-down and auto power-down
- Supports auto clock-gating mode
- Supports BIST
- Support single bank Refresh
- Support up to 12 Gbps @ TSMC N3P process
- Support high-performance scheduling and QoS

Applications

- Artificial Intelligence
- Machine Learning
- High-Performance Computing

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Digital Database	.gz

Note: the digital database contains RTL source code, synthesis constraint files, and simulation test bench

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