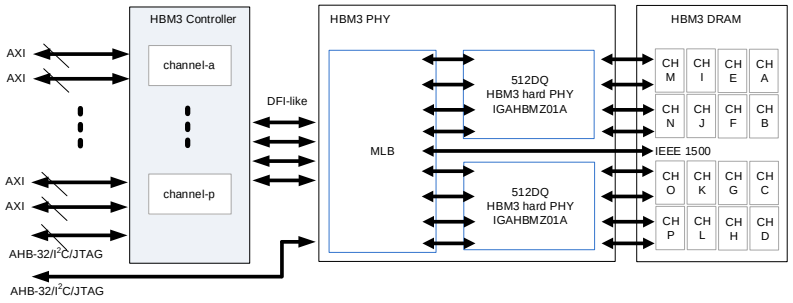
IGAHBMZ01A
TSMC CLN3FFE
HBM3 PHY

Overview

IGAHBMZ01A is a High Bandwidth Memory 3 Physical Layer (HBM3 PHY) compliant with JEDEC HBM3 DRAM Specification, JESD238. Built on TSMC 3 nm Enhanced process node, it supports the data rate of up to 8600 Mbps per data pin in the DFI-like 1:4 clock frequency ratio (HBM3 controller clock: WDQS = 1:4). The signal and power integrity are analyzed by the GUC design flow to meet all signal and power requirements.

GUC HBM3 PHY includes a hard PHY and an RTL soft module. The hard PHY, IGAHBMZ01A, includes command address modules, data modules, IO pads, PLL, and DLL. The RTL soft module, Miscellaneous Logic Block (MLB), is provided to work with the hard PHY for functions, such as the training logic, the register controller interface, the Built-In Self-Test (BIST) logic, and the IEEE 1500 function logic.



Block Diagram

Features

- HBM3 data rate: up to 8600 Mbps
- Supporting DFI-like 1:4 clock frequency ratio
  (HBM3 controller clock: WDQS = 1:4)
- Supporting only BL8
- Supporting AWORD/DWORD bus parity
- Supporting the programmable parity latency, PL = 0 and 2, of the DQ parity function
- Supporting HBM3 Data Bus Inversion (DBI)
- Supporting 64DQ ECC/SEV per channel
- HBM3 hard PHY delivered as a hard macro including IO, PLL, and DLL
- Supporting Internal Loopback and WRITE/READ BIST
- Supporting HBM3 loopback test, including MISR and LFSR modes
- Supporting IEEE 1500 Instruction
- Supporting HBM3 lane repairs with redundant pins for row/column/data
- Supporting HBM3 Duty Cycle Adjuster (DCA) and Duty Cycle Monitor (DCM)

Technology

- Process: TSMC 3 nm 0.75 V/1.2 V CMOS LOGIC FinFET Enhanced Process
- Special layer & device:
  SVT, LVT, LVTLL, ULVT, and ULVTLL
- Metal scheme: 1P17M
  (1Xa_h_1Xb_v_1Xc_h_1Xd_v_1Ya_h_1Yb_v_4Y_hvhv_4Yy2Z)

Applications

- For applications with high performance & high bandwidth memory, such as AI/HPC.

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4.	Testing Guide	.pdf
5.	PKG & PCB Guide	.pdf
6	Verilog Model	.v
7	Timing Model (LIB / DB)	.lib/.db
8	LEF Model	.lef
9	DRC/LVS/ANT/ERC Report	.rep
10	Netlist (Protected)	.spi
11	GDSII (Protected)	.gds

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC IP Eco-System provides the flexibility to work with IP from GUC, TSMC, and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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