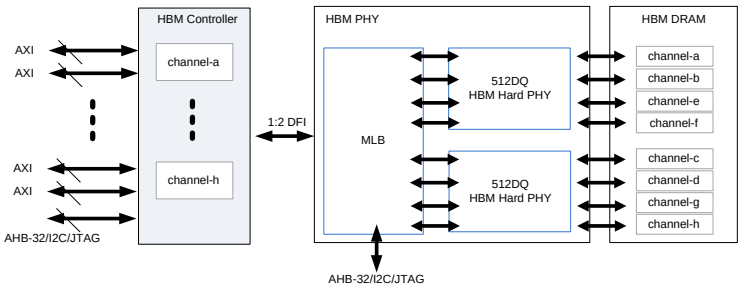
IGAHBMY02A
TSMC CLN5FF
HBM PHY IP

Overview

IGAHBMY02A is a High Bandwidth Memory (HBM) DRAM PHY IP, which complies to the JEDEC HBM2E & HBM2 standard. Three interfaces are provided to interface with controller, HBM DRAM, and configuration interface. DFI is the interface between HBM controller and PHY. HBM DRAM Spec. is the interface between HBM PHY and HBM DRAM. Configuration interfaces can be AHB, I^2C, and JTAG. Users can program HBM PHY configuration registers through this interface. HBM PHY includes two parts, MLB (miscellaneous logic blocks of PHY) and 512DQ PHY. Each 512DQ PHY includes one 4CA modules and eight 64DQ modules. 4CA module writes command to HBM DRAM, and 64DQ module writes and reads data to HBM DRAM. Two 512DQ PHY connect to HBM DRAM (8 channels).



Block Diagram

Features

- High Bandwidth Memory (HBM) DRAM PHY
- Supports HBM 3.6 Gbps
- Supports DFI 1:2
- Supports only BL4
- Supports AWORD/DWORD bus parity
- Supports programmable parity latency, PL = 0 and 2 , of DQ parity function
- Supports HBM data bus inversion (DBI) and write data mask (DM)
- Hard HBM PHY delivered as a hard macro component (includes I/O, PLL, and DLL)
- Supports HBM PHY internal loopback BIST
- Supports HBM lookback test, includes MISR and LFSR mode
- Supports IEEE 1500 instruction
- Supports HBM lane repairs with redundant pin for row/column/data

Technology

- Process: TSMC 5 nm 0.75 V/1.2 V CMOS LOGIC FinFET
- Special Layer & Device: (SVT, LVT, ULVT)
- Metal Scheme: 1P17M (1X_h_1Xb_v_1Xe_h_1Ya_v_1Yb_h_5Y_vhvhv_2Yy2Yx2R)

Applications

- For applications which need high performance & high bandwidth memory, such as AI/ HPC etc.

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4.	Testing Guide	.pdf
5.	PKG & PCB Guide	.pdf
6	Verilog Model	.v
7	Timing Model (LIB / DB)	.lib/.db
8	LEF Model	.lef
9	DRC/LVS/ANT/ERC Report	.rep
10	Netlist (Protected)	.spi
11	GDSII (Protected)	.gds
12	HBM PHY MLB RTL	RTL
13	HBM PHY MLB Script File	Script

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GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC's design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electro migration, dynamic IR drop and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all of GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC's IP Eco-System provides the flexibility to work with IP from GUC, TSMC and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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