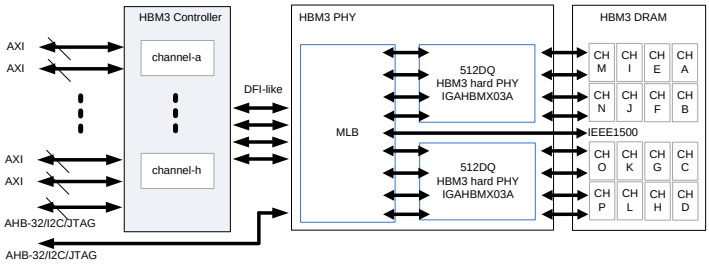
IGAHBMX03A
TSMC CLN7FF
HBM3 PHY

Overview

IGAHBMX03A is a HBM3 (High Bandwidth Memory) PHY IP compliant to the JEDEC HBM3 DRAM Specification Rev 0.95. Built on TSMC 7nm process node, it supports data rate up to 7200 Mbps per data pin with DFI 1:4 clock frequency ratio (controller clock : WCK = 1:4). Signal and power integrities were analyzed with GUC design flow to ensure all signal and power requirements could be met.

GUC HBM3 PHY IP includes both hard PHY and soft RTL module. The hard PHY IGAHBMX03A includes command address module, data module, IO pads, PLL and DLL. The soft RTL module MLB (miscellaneous logic block) is provided to work with hard PHY for functions such as training logic, register controller interface, BIST (Built-In Self-Test) logic and IEEE1500 function logic.



Block Diagram

Features

- HBM3 data rate up to 7200 Mbps
- Supports DFI-like 1:4 clock frequency ratio (controller clock : WCK = 1:4)
- Supports only BL8
- Supports AWORD/DWORD bus parity
- Supports programmable parity latency, PL=0 and 2 of DQ parity function
- Supports HBM3 data bus inversion (DBI)
- Supports 64DQ ECC/SEV per channel
- HBM3 hard PHY delivered as a hard macro which includes I/O, PLL, and DLL
- Supports internal loopback and READ/WRITE BIST
- Supports HBM3 loopback test, includes MISR and LFSR mode
- Supports IEEE 1500 instruction
- Supports HBM3 lane repairs with redundant pin for row/column/data
- Supports HBM3 duty cycle adjuster (DCA) and duty cycle monitor (DCM)

Technology

- Process: TSMC 7 nm 0.75 V/1.8 V CMOS LOGIC Fin FET Process
- Special Layer & Device: SVT, LVT, ULVT
- Metal Scheme: 1P15M (1X_h_1Xa_v_1Ya_h_5Y_vhvhv_2Y y2Yx2R)

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4.	Testing Guide	.pdf
5.	PKG & PCB Guide	.pdf
6	Verilog Model	.v
7	Timing Model (LIB / DB)	.lib/.db
8	LEF Model	.lef
9	DRC/LVS/ANT/ERC Report	.rep
10	Netlist (Protected)	.spi
11	GDSII (Protected)	.gds
12	HBM PHY MLB RTL	RTL
13	HBM PHY MLB Script File	Script

About Global Unichip Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC's design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electro migration, dynamic IR drop and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all of GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC's IP Eco-System provides the flexibility to work with IP from GUC, TSMC and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

For more information about this product or other GUC services please visit us on the web at www.guc-asic.com