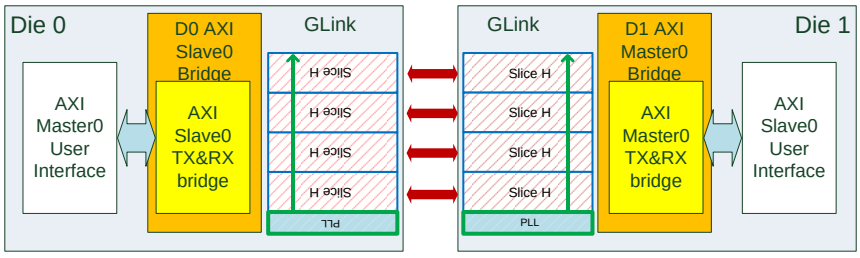
IGDD2D005A
GLink AXI-Bridge

Overview

GLink AXI-Bridge (IGDD2D005A) is a digital IP to interconnect between two dies which uses GLink as a physical layer and provides the AMBA AXI3/AXI4 compliant user interface bridged to each die. AXI-Bridge provides the data bus alignment between different applied GLink Slices to ensure consistent data could arrive at the AXI slave side. Due to AXI3/AXI4 spec supporting various data widths and signals, the amount of applied GLink Slices is dependent on the user AXI interface spec. GLink AXI-Bridge is a configurable design based on the user interface spec. By specifying AXI3/AXI4 interface signals with bit-width and some required the AXI interface configurations of one die, a specific GLink AXI-Bridge IP could be provided with the RTL code, timing constraints, and a test bench accordingly. GLink AXI-Bridge is compatible with GLink 2.x IP with PCS-replay enabled to ensure that no data errors could occur on GLink IP.



IGDD2D005A Block Diagram

Features

- Supports the AMBA AXI3/AXI4 compliant user interface
- Aligns data from multiple GLink Slices
- Compatible with any revisions of GLink IP with PCS-replay enabled
- Provides a pair of the AXI-Bridge IPs for Die-to-Die Data Transmission
- Supports multiple AXI channels merged to the same GLink Slice
- Clock latency of AXI TX Bridge is 0 or 1 clk_rx (default 1)
- Clock latency of AXI RX Bridge is 0 clk_tx
- Provides alignment fail status

Applications

- Provides AXI3/AXI4 bus interface and data bus alignment for occupied GLink Slices

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	RTL Source Code	.v
5	Synthesis Constraint File	.tcl
6	Simulation Test Bench	.v

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC IP Eco-System provides the flexibility to work with IP from GUC, TSMC, and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

For more information about this product or other GUC services please visit us on the web at www.guc-asic.com