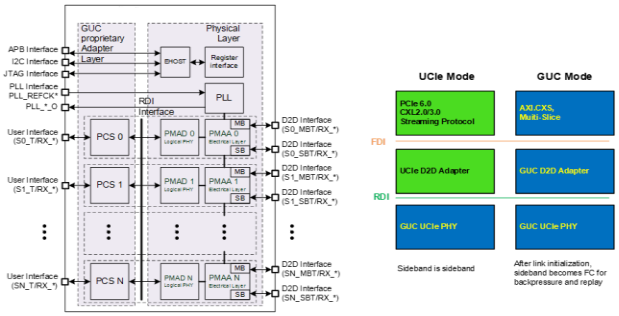
IGAD2DY08A

TSMC CLN5FF GUCIe LP Die-to-Die PHY

Overview

IGAD2DY08A is an LP (Low Power) Die-to-Die (D2D) PHY. This GUCIe PHY not only supports UCIe specification rev 1.1 compliance physical layer and Raw D2D interface (RDI) but also optionally provides the GUC proprietary Physical Coding Sublayer (PCS) to provide low-latency flow control for fast linked with AXI/CXS bus and provide error data replay (PCS-replay) feature to ensure the data transferred to RX is error-free. This IP is the UCIe Advanced package compliant that transmits data through TSMC advanced packaging solution at Chip-on-Wafer-on-Substrate (CoWoS®) with the Silicon and Redistribution Layer (RDL) interconnect interposer.

IGAD2DY08A contains 64 TX lanes and 64 RX lanes per module and supports the configurable number of modules up to eight in one PHY. Each TX/RX lane supports up to a 4/8/12/16/24/32/36 GT/s data rate. In summary, This IP offers a full-duplex data transmission with extremely low power and up to 2304 GT/s data rate per module in both directions. IGAD2DY08A contains the Electrical (Analog) Layer and Logical PHY Layer that support serialization, deserialization, link training, eye training, lane repair, lane reversal, scrambling and descrambling, sideband initialization and transfer, and clock forwarding functions. A Phase-Locked Loop (PLL) is also included.



IGAD2DY08A Block Diagram & GUCIe LP Support Modes

Features

- 32 GT/s UCIe compliance
- Max speed stretch to 36 GT/s
- 64 full-duplex lanes per module
- Support CoWoS-R/S/L
- Up to 8-module Analog PHY included in the analog hard macro
- UCIe RX matched length architecture
- Lane repair for Data, Valid, and CLK
- Built-in test pattern and checker
- EHOST: APB3, I²C, and JTAG register interface
- Power 0.41 pJ/bit @36GT/s
- Power 0.30 pJ/bit @24 GT/s
- 1.2 V analog supply voltage for PLL/Analog PHY and 0.75 V analog/digital supply voltage
- Independent low-power mode for analog blocks
- Operating junction temperature: -40 °C ~ 125 °C
- Marco size: 3304.23 µm (width) x 1234.21 µm (height) for NS orientation

Technology

- Process: TSMC 5 nm 0.75 V/1.2 V CMOS LOGIC FinFET Process
- Metal scheme: 1P16M (1P16M_1X_h_1Xb_v_1Xe_h_1Ya_v_1Yb_h_4Y_vhvh_2Yy2Yx2R)
- Special layer & device: N/A

Applications

- For applications with wired communications, such as AI and HPC.

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	PKG & PCB Guide	.pdf
6	Verilog Model	.v
7	Timing Model	.lib/.db
8	LEF Model	.lef
9	DRC/LVS/ANT/ERC/CNOD Report	.rep
10	Netlist (Flattened)	.spi
11	GDSII (Flattened)	.gds

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC IP Eco-System provides the flexibility to work with IP from GUC, TSMC, and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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