IGPD2DZ01A

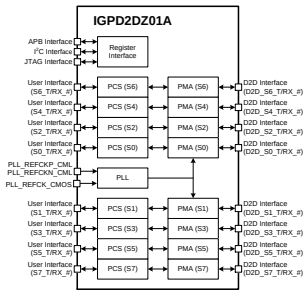
TSMC CLN3FFE GLink 2.3LL Die-to-Die PHY

Overview

IGPD2DZ01A is a high-speed Die-to-Die interface PHY that transmits data through TSMC advanced packaging solutions, Integrated Fan-Out (InFO) with the RDL interconnect, and Chip-on-Wafer-on-Substrate (CoWoS®) with the silicon interposer. IGPD2DZ01A contains 56 TX lanes and 56 RX lanes per slice and supports 8 slices in one PHY. Each TX/RX lane supports up to a 17.2 Gbps data rate. In summary, IGPD2DZ01A offers a full-duplex data transmission with extremely low power and up to 963.2 Gbps data rate per slice in both directions.

Each TX/RX slice contains PMA and PCS modules. PMA supports serialization, de-serialization, data transmission, eye training, and lane repair functions. PCS provides Data Bus Inversion (DBI), CRC/Parity Check, and FIFO Functions. A PLL is also included in IGPD2DZ01A to generate an 8.6 GHz high-speed clock for the data transmission.

IGPD2DZ01A is designed and fabricated in TSMC 3 nm FFE CMOS process with 1.2 V analog supply voltage for PLL/PMA and 0.75 V analog/digital supply voltages. Independent low power mode for PLL and slices is available.



IGPD2DZ01A Block Diagram

Features

- 56 full-duplex lanes per slice
- 6-Slice/2-Slice PMA included in the analog hard macro
- Lane repair
- Data Bus Inversion (DBI)
- CRC/Parity Check
- Built-in test pattern and checker
- EHOST: APB3, I²C, and JTAG register interface
- Built-in PLL
- 0.36 pJ/bit@17.2 Gbps power consumption
- 1.2 V analog supply voltage for PLL/PMA and 0.75 V analog/digital supply voltage
- Independent low power mode for analog blocks
- Operating junction temperature: -40 °C ~ 125 °C
- Marco size: 2309.376 µm (width) x 1426.048 µm (height) for 6-Slice vertical macro and 892.416 µm (width) x 1426.048 µm (height) for 2-Slice vertical macro

Technology

- Process: TSMC 3 nm 0.75 V/1.2 V CMOS LOGIC FinFET Enhanced Process
- Metal scheme: 1P17M (1Xa_h_1Xb_v_1Xc_h_1Xd_v_1Ya_h_1Yb_v_4Y_hvhv_4Yy2Z)
- Special layer & device: N/A

Applications

- Die-to-Die interface

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	PKG & PCB Guide	.pdf
6	Verilog Model	.v
7	Timing Model	.lib/.db
8	LEF Model	.lef
9	DRC/LVS/ERC/ANT Report	.rep
10	Netlist (Flattened)	.spi
11	GDSII (Flattened)	.gds

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GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC IP Eco-System provides the flexibility to work with IP from GUC, TSMC, and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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