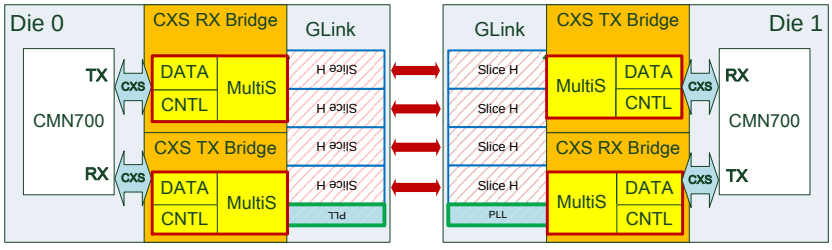
IGDD2D006A
GLink CXS-Bridge

Overview

GLink CXS-Bridge (IGDD2D006A) is a digital IP to interconnect between two dies which uses GLink as a physical layer and provides the AMBA CXS issue-B compliant user interface bridged to each die. CXS-Bridge provides the data bus alignment between different applied GLink Slices to ensure consistent data could arrive at the CXS RX interface. Due to CXS properties defining various data width and control signals, the amount of applied GLink Slices is dependent on the user-specified spec. GLink CXS-Bridge is a configurable design based on the user interface spec. By specifying CXS properties and some required the CXS interface configurations of one die, a specific GLink CXS-Bridge IP could be provided with the RTL code, timing constraints, and a test bench accordingly. GLink CXS-Bridge is compatible with GLink 2.x IP with PCS-replay enabled to ensure that no data errors could occur on GLink IP.

GLink CXS-Bridge Properties

CXS Property	GLink CXS-Bridge
CXS_LAST	True
CXS_MAX_CREDIT	4
CXS_MAX_CREDIT_LATENCY	TX: 1, RX: 1
CXS_PROTOCOL_TYPE	True
CXSCHECKTYPE	None
CXSERRORFULLPKT	False
CXSLINKCONTROL	Explicit_Credit_Return
CXSCONTINUOUSDATA	False
CXSDATAFLITWIDTH	256 / 512 / 1024
CXSMAXPKTPERFLIT	2 / 3 / 4



Block Diagram

Features

- Provides the AMBA CXS issue-B compliant user interface
- Aligns data from multiple GLink Slices
- Compatible with any revisions of GLink IP with PCS-replay enabled
- Provides a pair of the CXS-Bridge IPs for the Die-to-Die Data Transmission
- Supports Explicit_Credit_Return property
- Supports Explicit_Credit_Return property to handle the activation and the deactivation
- Clock latency of CXS TX bridge is 0 or 1 clk_rx (default 1)
- Clock latency of CXS RX bridge is 0 clk_tx
- Provides alignment fail status

Applications

- Provides CXS issue-B UI and data alignment for GLink 2.5D series

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	RTL Source Code	.v
5	Synthesis Constraint File	.tcl
6	Simulation Test Bench	.v

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC IP Eco-System provides the flexibility to work with IP from GUC, TSMC, and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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