IGAD2DX01A

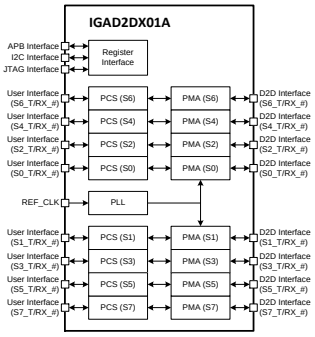
TSMC CLN6FF/CLN7FF Die-to-Die Interface PHY

Overview

IGAD2DX01A is a high speed die-to-die interface PHY which transmits data through InFO_oS or CoWoS channels. IGAD2DX01A contains 32 Tx lanes and 32 Rx lanes per slice and supports 8 slices in one PHY. Each Tx/Rx lane can support up to 8 Gbps data rate. In summary, IGAD2DX01A offers a full-duplex data transmission with extremely low power and up to 256 Gbps data rate per slice in both directions.

Each Tx/Rx slice contains PMA and PCS modules. PMA supports serialization, de-serialization, data transmission, eye training and lane repair functions. PCS provides data bus inversion, parity check and FIFO functions. One PLL is also included in IGAD2DX01A to generate 8 GHz high speed clock for data transmission.

IGAD2DX01A is designed and fabricated in TSMC 7 nm/6 nm FF CMOS process with 1.8 V analog supply voltage for PLL and 0.75 V analog/digital supply voltages. Independent power down mode for PLL and slices is available.



IGAD2DX01A Block Diagram

Features

- 32 full-duplex lanes per slice
- 8 slices are included in analog hard macro
- Lane repair
- Data bus inversion
- Parity check
- Built-in test pattern and checker
- EHOST : APB , I^2C, and JTAG register interface
- Built-in PLL
- 0.25 pJ/bit power consumption
- 1.8 V analog supply voltage for PLL and 0.75 V analog/digital supply voltage
- Independent power down mode for analog blocks
- Operating junction temperature: -40 ^oC ~ 125 ^oC
- Analog hard macro size: 690 um x 3037.44 um (2.096 mm2) for horizontal macro and 3037.074 um x 690 um (2.096 mm^2) for vertical macro (pre-shrink)

Technology

- Process: TSMC 6 nm 0.75 V/1.8 V CMOS LOGIC FinFET Process or TSMC 7 nm 0.75 V/1.8 V CMOS LOGIC FinFET Process
- Metal Scheme : 1P13M (1X_h_1Xa_v_1Ya_h_5Y_vhvhv_2Yy2Z)) or 1P15M (1X_h_1Xa_v_1Ya_h_5Y_vhvhv_2Yy2Yx2R
- Special Layer & Device Type : High R Resistance, ULVT

Applications

- Die-to-die interface

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	Verilog Model	.v
6	Timing Model	.lib/.db
7	LEF Model	.lef
8	DRC/LVS/ERC/ANT Report	.rep
9	Netlist (Flattened)	.spi
10	GDSII (Flattened)	.gds
11	Integration checklist	.xlsx
12	Digital Database (Protected)	.gz
13	Evaluation Kit	.gz
14	License Key(For Evaluation Kit)	.vp

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GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC's design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electro migration, dynamic IR drop and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all of GUC's IPs are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC's IP Eco-System provides the flexibility to work with IP from GUC, TSMC and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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