IGAD2DY04A

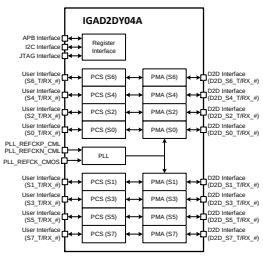
TSMC CLN5FF GLink 2.3LL Die-to-Die PHY

Overview

IGAD2DY04A is a high-speed die-to-die interface PHY which transmits data through TSMC advanced packaging solutions: Integrated Fan-Out (InFO) with RDL interconnect and Chip-on-Wafer-on-Substrate (CoWoS®) with silicon interposer. IGAD2DY04A contains 56 TX lanes and 56 RX lanes per slice and supports 8 slices in one PHY. Each TX/RX lane can support up to 17.2 Gbps data rate. In summary, IGAD2DY04A offers a full-duplex data transmission with extremely low power and up to 963.2 Gbps data rate per slice in both directions.

Each TX/RX slice contains PMA and PCS modules. PMA supports serialization, de-serialization, data transmission, eye training, and lane repair functions. PCS provides data bus inversion (DBI), CRC check, and FIFO functions. One PLL is also included in IGAD2DY04A to generate an 8.5 GHz high-speed clock for data transmission.

IGAD2DY04A is designed and fabricated in TSMC 5 nm FF CMOS process with 1.2 V analog supply voltage for PLL/PMA and 0.75 V analog/digital supply voltages. Independent low power mode for PLL and slices is available.



IGAD2DY04A Block Diagram

Features

- 56 full-duplex lanes per slice
- 8 slices are included in analog hard macro.
- Lane repair
- Data bus inversion
- CRC check
- Built-in test pattern and checker
- Programming interface APB, I^2C, and JTAG
- Built-in PLL
- ~0.3 (TBD) pJ/bit power consumption
- 1.2 V analog supply voltage for PLL/PMA and 0.75 V analog/digital supply voltage
- Independent low power mode for analog blocks
- Operating junction temperature: -40 °C ~ 125 °C
- IP GDS size: 3050 µm x 1076 µm (3.281 mm^2) for North-South direction macro and 1113 µm x 3050 µm (3.39 mm^2) for East-West direction macro

Technology

- Process: TSMC 5 nm 0.75 V/1.2 V CMOS LOGIC FinFET Process
- Metal Scheme: 1P17M (1X_h_1Xb_v_1Xe_h_1Ya_v_1Y b_h_5Y_vhvhv_2Yy2Yx2R)
- Special Layer & Device: High R Resistance, ULVT

Applications

- Die-to-Die interface

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	PKG & PCB Guide	.pdf
6	Verilog Model	.v
7	Timing Model	.lib/.db
8	LEF Model	.lef
9	DRC/LVS/ERC/ANT Report	.rep
10	Netlist (Flattened)	.spi
11	GDSII (Flattened)	.gds

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC IP Eco-System provides the flexibility to work with IP from GUC, TSMC, and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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