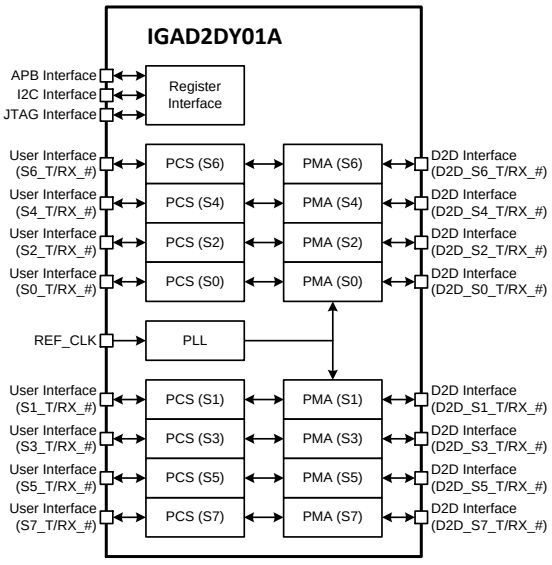
IGAD2DY01A

TSMC CLN5FF GLink-fs 2.0 Die-to-Die PHY

Overview

IGAD2DY01A is a high speed die-to-die interface PHY which transmits data through INFO RDL channels. IGAD2DY01A contains 32 Tx lanes and 32 Rx lanes per slice and supports 8 slices in one PHY. Each Tx/Rx lane can support up to 16 Gbps data rate. In summary, IGAD2DY01A offers a full-duplex data transmission with extremely low power and up to 512 Gbps data rate per slice in both directions.

IGAD2DY01A is designed and fabricated in TSMC 5 nm FF CMOS process with 1.2 V analog supply voltage for PLL and 0.75 V analog/digital supply voltages. Independent power-down mode for PLL and slices is available.



IGAD2DY01A Block Diagram

Features

- 32 full-duplex lanes per slice
- 8 slices are included in analog hard macro
- Lane repair
- Data bus inversion
- CRC/Parity check
- Built-in test pattern and checker
- Programming interface APB , I^2C, and JTAG
- Built-in PLL
- 0.308 pJ/bit power consumption
- 1.2 V analog supply voltage for PLL and 0.75 V analog/digital supply voltage
- Independent low power mode for analog blocks
- Operating junction temperature: -40 °C ~ 125 °C
- IP GDS size:746.283 um x 3047.268 um (2.274 mm^2) for horizontal macro and 3048.576 um x 744.968 um (2.271 mm^2) for vertical macro

Technology

- Process: TSMC 5 nm 0.75 V/1.2 V CMOS LOGIC FinFET Process
- Metal Scheme : 1P16M (1X_h_1Xb_v_1Xe_h_1Ya_v_1Y b_h_4Y_vhvh_2Yy2Yx2R)
- Special Layer & Device : High R Resistance, ULVT

Applications

- Die-to-die interface

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	PKG & PCB Guide	.pdf
6	Verilog Model	.v
7	Timing Model	.lib/.db
8	LEF Model	.lef
9	DRC/LVS/ERC/ANT Report	.rep
10	Netlist (Flattened)	.spi
11	GDSII (Flattened)	.gds

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC's design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electro migration, dynamic IR drop and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all of GUC's IPs are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC's IP Eco-System provides the flexibility to work with IP from GUC, TSMC and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

For more information about this product or other GUC services please visit us on the web at www.guc-asic.com