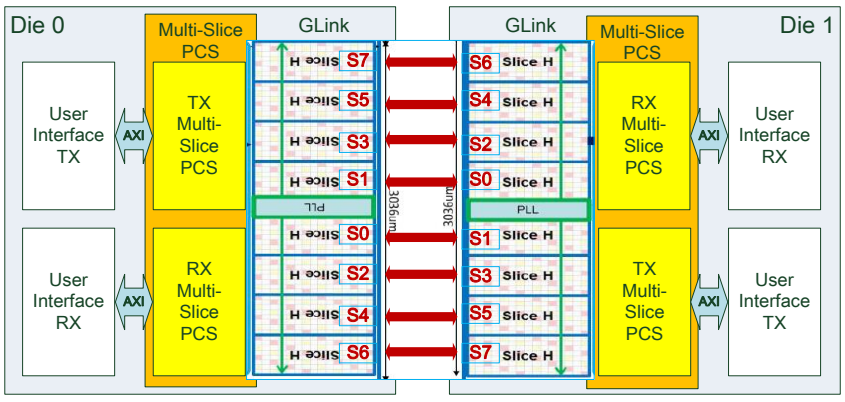
IGDD2D004A

GLink Multi-Slice PCS

Overview

GLink (GLink-fs 2.x + PCS-replay) Multi-Slice PCS is a digital IP designed to provide data bus alignment between different applied GLink Slices to ensure consistent data could arrive at the RX side. GLink Multi-Slice PCS is a configurable design based on user configuration. By specifying information such as number of user interfaces, relative data bus width, whether different user interfaces will be merged into one GLink Slice and the user interface frequency information, a specific GLink Multi-Slice PCS design could be generated which include RTL code with timing constraints and a testbench. The Multi-Slice PCS is compatible with GLink 2.x IP which equip with PCS-replay feature to ensure that no data error would occur on GLink IP.



Block Diagram

Features

- Align data buses of different GLink Slices
- Compatible with any revision of GLink IP with PCS-replay feature
- VALID and READY handshake mechanism
- Support any data bus width
- Support multiple user interface data buses merging into a single GLink Slice
- Support up to eight combined Slices
- Provide pairing of TX and RX Multi-Slice PCS
- Provide option for symmetrical duplex transaction between Dies
- TX Multi-Slice PCS latency is default to 0 TX clock
- RX Multi-Slice PCS latency is default to 1 RX clock
- Provide alignment failure status indication

Applications

- Provide data bus alignment for different GLink Slices

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	RTL Source Code	.v
5	Synthesis Constraint File	.tcl
6	Simulation Test Bench	.v

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC's design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electro migration, dynamic IR drop and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all of GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC's IP Eco-System provides the flexibility to work with IP from GUC, TSMC and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

For more information about this product or other GUC services please visit us on the web at www.guc-asic.com