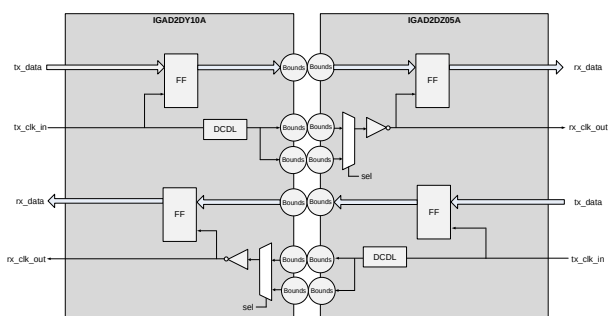


IGAD2DZ05A IGAD2DY10A TSMC CLN3FFP/CLN5FF GLink-3D Die-to-Die PHY Overview

IGAD2DY10A and IGAD2DZ05A are both GLink-3D high-speed Die-to-Die interface PHY IPs. IGAD2DY10A is the Primary (Master) PHY IP and IGAD2DZ05A is the Secondary (Slave) PHY IP. Each IP is used to transmit data between dies through TSMC System on Integrated Chips (SoIC-X) 3D stacking technology (3DFabric), which supports Chip-on-wafer (CoW) assembly, with face-to-face die stacking. IGAD2DY10A and IGAD2DZ05A communicate with each other and are both constructed with TX and RX data blocks in a complete macro. These two IPs share the same architecture and have a symmetrical physical layout floorplan. The data lanes transfer at a bit rate of 1.6 Gbps at 0.6 V operating range and 2.2 Gbps at 0.85 V operating range in one direction.

Each IP contains PMAD and PMAA modules. PMAA supports data transmission with an SDR interface on data bits. PMAD provides parity generation, checker, and lane repair functions. PMAD also provides full Scan support, Loopback, BIST generator, and checker.



IGAD2DY10A/IGAD2DZ05A Block Diagram

Features

- Supports SoIC-X (3DFabric) CoW assembly
- Supports face-to-face die stacking
- Supports point-to-point communication between single Primary and single Secondary
- Data rate per bond: 1.6 Gbps at 0.6 V +/-10 % and 2.2 Gbps at 0.85 V +/-10 %
- TX/RX lanes transfer in SDR manner
- Implemented with 130 TX and 130 RX data lanes
- Include 1 bit for parity generation and checking for TX and RX respectively
- Include 4 bits for data lanes repair for TX and RX respectively (2 redundant lanes cover 65 data lanes) and 2 bits for clock lane repair
- 0.05 pJ/bit power consumption
- Supports internal loopback mode, far-end loopback modes, Scan, and BIST
- Supports programming by sideband channel between different dies
- The IP can be configured by APB, I²C, or JTAG interfaces

Technology

- Process:
IGAD2DZ05A: TSMC 3 nm 0.75 V/1.2 V CMOS LOGIC FinFET Advanced Process
IGAD2DY10A: TSMC 5 nm 0.75 V/1.2 V CMOS LOGIC FinFET Process
- Special Layer & Device: SoIC-X related layers
- Metal Scheme:
IGAD2DZ05A: 1P18M
(1Xa_h_1Xb_v_1Xc_h_1Xd_v_1Ya_h_1Yb_v_5Y_hvvhv_2Yy2Yx2R)
IGAD2DY10A: 1P16M
(1X_h_1Xb_v_1Xe_h_1Ya_v_1Yb_h_4Y_vhvh_2Yy2Yx2R)

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Verilog Model	.v
5	Timing Model	.lib/.db
6	LEF Model	.lef
7	DRC/LVS/ERC/ANT/CNOD Report	.rep
8	Netlist (Flattened)	.spi
9	GDSII (Flattened)	.gds
10	DFT CTL Model	.ctl
11	CPM Model	.sp
12	IP-XACT file and RAL model	.xml/.sv

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC IP Eco-System provides the flexibility to work with IP from GUC, TSMC, and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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