IGAD2DX03A

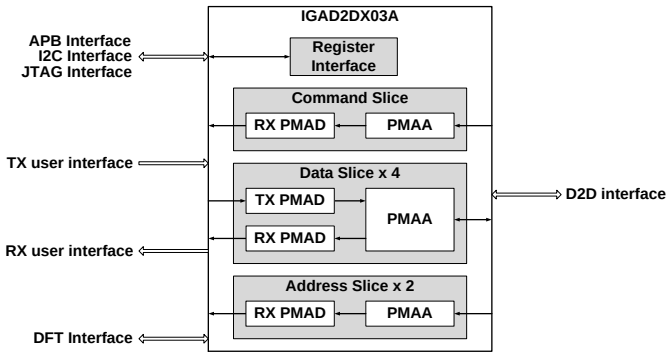
TSMC CLN7FF

GLink-3D Die-to-Die Slave PHY

Overview

IGAD2DX03A is a GLink-3D high speed die-to-die interface Slave PHY. It is used to transmit data between dies and assembled using TSMC System on Integrated Chips (SoIC) 3D stacking technology (3DFabric). The IP supports both Wafer-on-wafer (WoW) and Chip-on-wafer (CoW) assembly with both face to face and face to back options. It is used to communicate with IGAD2DY02A (Master PHY). Both IGAD2DY02A and IGAD2DX03A are built with TX and RX Data and Command Slices in a modular way. Each Data Slice allows transferring 16 bits at bit rate of 5.0 Gbps in one direction, totaling 80 Gbps per Data Slice.

The IP contains PMAD and PMAA modules. PMAA supports data transmission with DDR interface on data/address slice and SDR interface on command slice. PMAD provides parity generation and checker plus lane repair functions. PMAD also provides full Scan support, Loopback, BIST generator and checker plus data training with IGAD2DY02A (Master PHY).



IGAD2DX03A Block Diagram

Features

- Supports SoIC (3DFabric) CoW and WoW assembly
- Supports face to face and face to back with the same GDSII
- Supports point to multi-point (multi-Slave) communication
- Up to 5 Gbps/bond (2.5 GHz DDR) data rate
- 16 TX/RX lanes/data slice and 16 RX lanes/address slice (DDR)
- 14 RX lanes/command slice (SDR)
- Supports 4 TX and 4 RX data slices, 2 address slices and 1 command slice
- Latency of TX: 1T and RX: 1T
- Power consumption: 0.182pj/bit
- Supports Parity generation and checking plus Lane repair
- Supports Read, Write and multi-Slave BIST
- Supports loopback and SCAN
- IP can be configured by APB, I^2C, or JTAG interfaces

Technology

- Process: TSMC 7 nm 0.75 V/1.8 V CMOS LOGIC Fin FET
- Special Layer & Device: SoIC related layers; LVT and ULVT
- Metal Scheme: 1P13M (2X_hv_1Ya_h_5Y_vhvhv_2Yy2R)

Applications

- Die-to-die interface for 3DIC

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	Verilog Model	.v
6	Timing Model	.lib/.db
7	LEF Model	.lef
8	DRC/LVS/ANT/ERC Report	.rep
9	Netlist (Flattened)	.spi
10	GDSII (Flattened)	.gds
11	Digital Database (Protected)	.gz

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC's design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electro migration, dynamic IR drop and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all of GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC's IP Eco-System provides the flexibility to work with IP from GUC, TSMC and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.**For more information about this product or other GUC services please visit us on the web at www.guc-asic.com**