IGAADCX04A

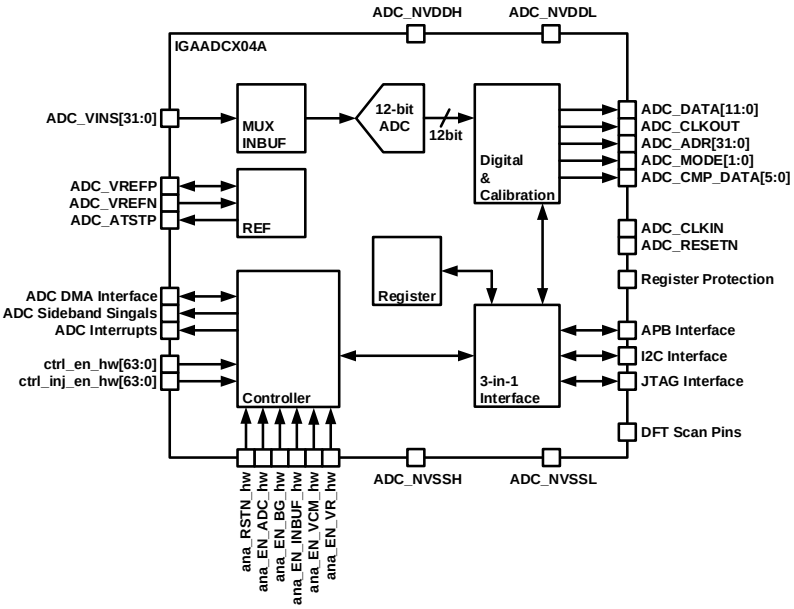
TSMC CLN7FF 12-bit 16 Msps SAR ADC [32ch]

Overview

IGAADCX04A is a general-purpose analog-to-digital converter (ADC) with a 12-bit resolution and a 32-to-1 input multiplexer. The sampling rate is up to 16 MHz. The converted digital code is represented by an unsigned binary format.

IGAADCX04A contains a 12-bit SAR ADC, an ADC controller, and a foreground calibration module, and supports 3-in-1 (I^2C/JTAG/APB) interfaces to achieve the functionality configuration and output acquisition.

A power-down mode is available to disable ADC and for lower power dissipation.



IGAADCX04A Block Diagram

Features

- 12-bit resolution
- INL: < +/-4.0 LSB, DNL: < +/-2.0 LSB
- Sampling rate: up to 16 MHz
- Single-end input sampling
- Supply voltage:
  1.8 V for analog
  0.75 V for digital
- Unsigned binary format
- Supports I^2C, JTAG, and APB interface
- Power-down mode available
- Operating junction temperature:
  -40 °C to 125 °C
- Macro size:
  800 µm (width) x 300 µm (height)

Technology

- Process: TSMC 7 nm 0.75 V/1.8 V CMOS LOGIC FinFET Process
- Special layer & device:
  - Core device:
    nch_svt / pch_svt / nch_lvt / pch_lvt / nch_ulvt / pch_ulvt
  - IO device: nch_18 / pch_18
  - High-R resistor: rhim
  - BJT: PNP
  - RTMOM
- Metal scheme: 1P8M
  (1X_h_1Xa_v_1Ya_h_4Y_vhvh)

Applications

- Data Acquisition system

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	Verilog Model	.v
6	Timing Model	.lib/.db
7	LEF Model	.lef
8	DRC/LVS/ERC/ANT Report	.rep
9	Netlist (Flattened)	.spi
10	GDSII (Flattened)	.gds
11	Integration Checklist	.xlsx
12	Netlist (Phantom) (optional)	.spi
13	GDSII (Phantom) (optional)	.gds
14	IBIS Model (optional)	.ibs
15	DFT Pattern	.tgz
16	SDF and Post-APR Netlist	.tgz
17	Reference Document (optional)	.pdf
18	CPM Model (optional)	.tgz

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GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC IP Eco-System provides the flexibility to work with IP from GUC, TSMC, and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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