

IGAAFEV03A

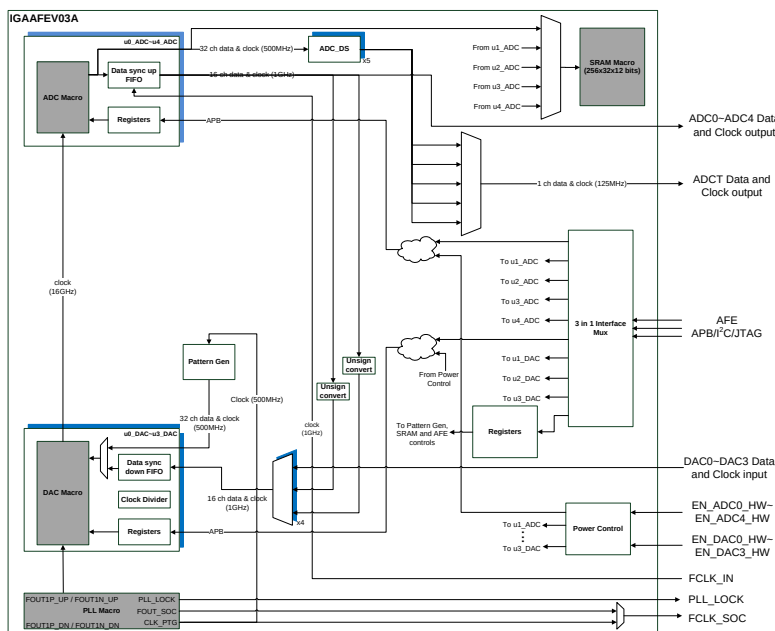
TSMC CLN12FFC

16 Gsps Analog Front-End

Overview

IGAAFEV03A is a high speed analog front-end circuit for 5GNR application which supports 4T4R. IGAAFEV03A contains five 12 bit 16 Gsps SAR ADCs, four 12 bit 16 GHz DACs and one 16 GHz PLL. IGAAFEV03A support I²C, JTAG, and APB 3-in-1 interface to handle configuration and functionality control for ADC, DAC, and PLL. Individual power-down mode of each ADC, DAC, and PLL is built in for power consumption reduction.

IGAAFEV03A is designed and fabricated in TSMC 12 nm FF CMOS process.



IGAAFEV03A Block Diagram

Features

- Support 4T4R
- 12 bit 16 Gsps ADC
- 12 bit 16 Gsps DAC
- 16 GHz PLL
- Build in 16 GHz clock input bypass mode
- SoC interface data rate: 1 GHz
- Built-in pattern generator for DAC testing
- Built-in SRAM, and down sample for ADC test
- EHOST: APB, I²C, and JTAG register interface
- Operating junction temperature: -40 °C ~ 125 °C
- Build in individual power-down mode for each ADC, DAC, and PLL
- 1.8 V/0.9 V analog supply voltage and 0.8 V digital supply voltage
- IP GDS size: 1500 um (Width) x 8000 um (Height)

Technology

- Metal Scheme: 1P9M (2Xa1Xd_h_3Xe_vhv_2Z) + UT-ALRDL
- Process: TSMC 12 nm 0.8 V/1.8 V CMOS LOGIC FinFET Compact
- Special Layer & Device: DNW, High-R Resistor, ulvt, MOM cap, SRAM

Applications

- 5GNR analog front-end

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	Verilog Model	.v
6	Timing Model	.lib/.db
7	LEF Model	.lef
8	DRC/LVS/ERC/ANT Report	.rep
9	Netlist (Flattened)	.spi
10	GDSII (Flattened)	.gds
11	Integration Checklist	.xlsx
12	DFT	.tgz
13	SDF and Post-APR Netlist	.tgz
14	Netlist (Phantom)	.spi
15	GDSII (Phantom)	.gds
16	IBIS Model	.ibs
17	Reference Document	.pdf

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC's design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electro migration, dynamic IR drop and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all of GUC's IPs are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC's in-house IP Portfolio includes DDR, High Speed Interface, Data Converter, Hardened ARM Core, Multimedia and specialized IP. GUC's IP Eco-System provides the flexibility to work with IP from GUC, TSMC and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

For more information about this product or other GUC services please visit us on the web at www.guc-asic.com