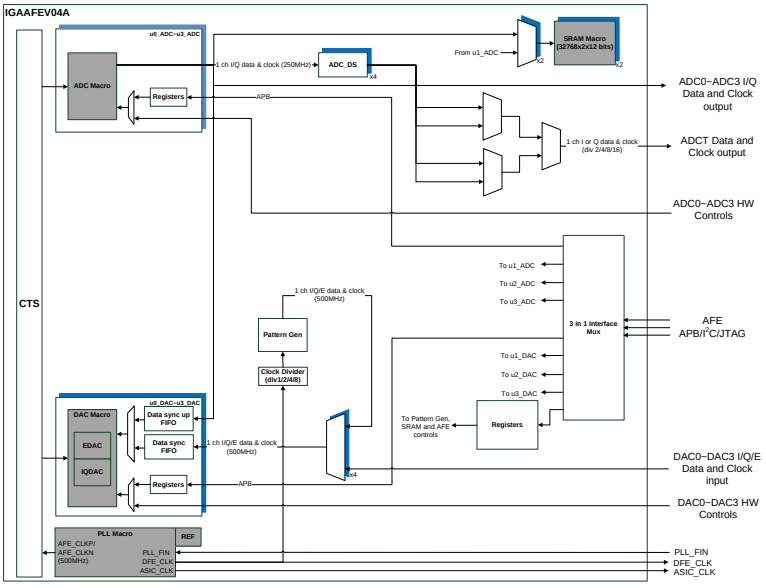
IGAAFEV04A

TSMC CLN12FFC 500 MHz Analog Front-End

Overview

IGAAFEV04A is a 500 MHz analog front-end circuit. IGAAFEV04A contains four 12 bit 250 MHz SAR 2-channel ADCs, four 12 bit 500 MHz Current Steering 3-channel DACs and one 500 MHz General-Purpose PLL. IGAAFEV04A support I^{2}C, JTAG, and APB 3-in-1 interface to handle configuration and functionality control for ADC, DAC, and PLL. Individual power-down mode of each ADC, DAC, and PLL is built in for power consumption reduction.

IGAAFEV04A is designed and fabricated in TSMC 12 nm FF CMOS process.



IGAAFEV04A Block Diagram

Features

- SoC Interface Data rate: 500 MHz
- Built-in pattern generator for DAC testing
- Built-in SRAM, and down sample for ADC testing.
- EHOST: APB, I^{2}C, and JTAG register interface.
- 1.8 V/0.9 V analog supply voltage and 0.8 V digital supply voltage
- Build in individual power-down mode for each ADC, DAC, and PLL
- Operating junction temperature: -40 °C ~ 125 °C
- IP GDS size: 960 µm (Width) x 4600 µm (Height)
- 2-ch 12 bit 250 MHz SAR ADC
- 3-ch 12 bit 500 MHz Current Steering DAC
- 500 MHz general-purpose PLL

Technology

- Process: TSMC 12 nm 0.8 V/1.8 V CMOS LOGIC FinFET Compact Process
- Metal Scheme : 1P9M (2Xa1Xd_h_3Xe_vhv_2Z) + UT-ALRDL
- Special Layer & Device Type : DNW, High-R Resistor, ulvt, MOM cap, SRAM

Applications

- Analog base band

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	Verilog Model	.v
6	Timing Model	.lib/.db
7	LEF Model	.lef
8	DRC/LVS/ERC/ANT Report	.rep
9	Netlist (Flattened)	.spi
10	GDSII (Flattened)	.gds
11	Integration Checklist	.xlsx
12	DFT	.tgz
13	SDF and Post-APR Netlist	.tgz
14	Netlist (Phantom) (optional)	.spi
15	GDSII (Phantom) (optional)	.gds
16	IBIS model (optional)	.ibs
17	Reference Document (optional)	.pdf

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GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC's design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electro migration, dynamic IR drop and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all of GUC's IPs are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC's IP Eco-System provides the flexibility to work with IP from GUC, TSMC and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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