IGAPLLV10A

TSMC CLN12FFC Spread Spectrum PLL

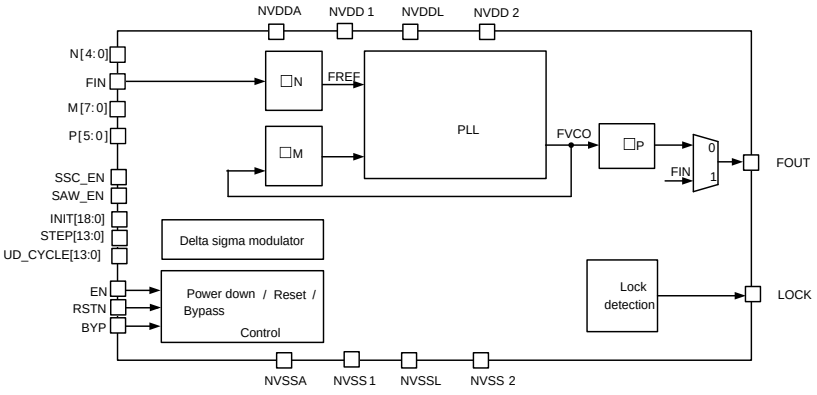
Overview

IGAPLLV10A is the Spread Spectrum Phase-Locked Loop (SSPLL) without external components and is designed to provide a stable and accurate clock. There is a lock detection function and a robust VCO architecture in the SSPLL.

IGAPLLV10A generates an output clock (25 MHz ~ 3600 MHz) from the input clock (7.5 MHz ~ 200 MHz). The spread spectrum modulation frequency is up to 100 kHz.

The SSPLL integrates a voltage-controlled oscillator, a phase frequency detector, a charge pump, a loop filter, three frequency dividers, and a delta-sigma modulator for spread spectrum control. The clock generator circuit incorporates bypass and power-down modes for power saving.

IGAPLLV10A is designed for TSMC 12 nm CMOS Logic FinFET Compact 1P7M (2Xa1Xd_h_3Xe_vhv) 0.8 V/1.8 V process.



IGAPLLV10A Block Diagram

Features

- Lock detection function
- 1.8 V analog supply operation and 0.8 V digital supply operation
- Input clock frequency range: 7.5 MHz to 200 MHz
- Output clock frequency range: 25 MHz to 3600 MHz
- Spread spectrum modulation frequency selection control
- Spread spectrum spread ratio control
- Spread spectrum on/off control
- Fractional mode on/off control
- Fully integrated PLL without external loop filters
- Power-down capability
- Bypass mode
- Macro size: 270 µm (width) x 300 µm (height)
- Operating junction temperature: -40 °C ~ 125 °C

Technology

- Process: TSMC 12 nm 0.8 V/1.8 V CMOS LOGIC FinFET Compact Process
- Metal scheme: 1P7M (2Xa1Xd_h_3Xe_vhv)
- Special layer & device: ULVT & High-R Resistor: rhim

Applications

- Clock Generator

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	Verilog Model	.v
6	Timing Model	.lib/.db
7	LEF Model	.lef
8	DRC/LVS/ERC/ANT Report	.rep
9	Netlist (Flattened)	.spi
10	GDSII (Flattened)	.gds
11	Integration Checklist	.xlsx
12	Netlist (Phantom) (optional)	.spi
13	GDSII (Phantom) (optional)	.gds
14	IBIS Model (optional)	.ibs
15	Reference Document (optional)	.pdf

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As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

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