IGAPLLX03A

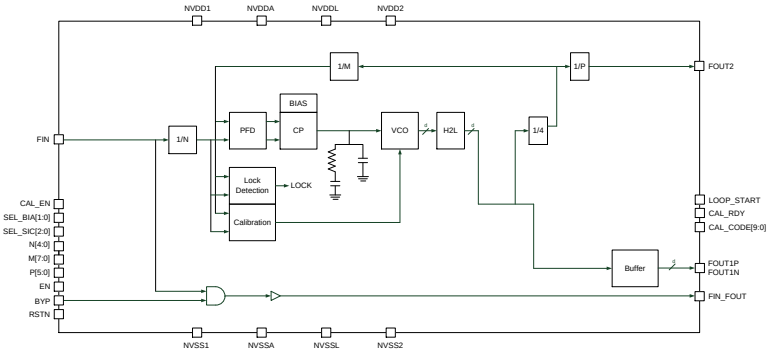
TSMC CLN7FFC General Purpose LC PLL

Overview

IGAPLLX03A is a general-purpose Phase-Locked Loop (PLL) with external low pass filter capacitor C (2.4 nF). It is designed to provide a stable and accurate clock for high speed and high resolution ADC. The PLL has bypass mode function. The bypass mode can bypass high speed (16 GHz) clock from PLL input to PLL output.

This PLL IP optimizes the phase jitter performance with the limited current consumption.

IGAPLLX03A is LC tank type PLLs. The LC PLL frequency is 16 GHz in usual case. The PLL incorporates several frequency dividers to generate various output frequencies for different applications. For PVT variation, the PLL has auto frequency calibration function in normal operating mode. The power-down mode is available to shut down the power of the PLL circuit. IGAPLLX03A is designed for TSMC CLN7FF 0.75 V/1.8 V process.



IGAPLLX03A Block Diagram

Features

- 1.8 V analog supply operation and 0.75 V/0.9 V digital supply operation
- Frequency calibration function
- Power-down mode
- Bypass mode.
- Lock detection function.
- IP GDS size: x = 400 um, y = 620 um
- Operating Junction temperature: -40 ˚C ~125 ˚C

Technology

- Process: TSMC 7 nm 0.75 V/1.8 V CMOS LOGIC FinFET Process
- Special Layer & Device: High-R Resistor, ulvt, MOM cap ,inductor, varactor, BJT
- Metal Scheme : 1P13M (1X_h_1Xa_v_1Ya_h_5Y_vhvhv_2Yy2R)

Applications

- PLL

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	Verilog Model	.v
6	Timing Model	.lib/.db
7	LEF Model	.lef
8	DRC/LVS/ERC/ANT Report	.rep
9	Netlist (Flattened)	.spi
10	GDSII (Flattened)	.gds

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