GUC
The Advanced ASIC Leader

IGATHMX02A

TSMC CLN7FF
Thermal Sensor ADC

Release Note
Version: v024
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Revision History

Version	Date	Remarks
v001	Mar. 26, 2019	Preliminary
v002	Apr. 25, 2019	Add front-end and back-end model
v003	May 23, 2019	Update LIB and datasheet
v004	Jun. 11, 2019	Update VLG
v005	Jun. 17, 2019	Update LIB header
v006	Aug. 14, 2019	Update THMD connection and relative model
v007	Sept. 10, 2019	Update LIB, datasheet, and ATE testing guide
v008	Oct. 08, 2019	Update LIB and datasheet
v009	Nov. 17, 2020	Update mapping table in datasheet and VLG Update the dependency table.
v010	Jun. 01, 2021	Update datasheet and integration checklist
v011	Jan. 07, 2022	Update quality grade to be silicon proven
v012	Mar. 27, 2022	(1) Update GDS and phantom GDS for IP_TAG correction (2) Update DRC/LVS/ERC/ANT report
v013	May 04, 2022	Update datasheet and product brief.
v014	Jul. 07, 2022	Add a new metal scheme
v015	Jul. 29, 2022	Update VLG
v016	Aug. 15, 2022	Update VLG for ECO (clock output) behavior
v017	Feb. 01, 2023	Update datasheet and integration checklist
v018	Jan. 23, 2024	Update datasheet
v019	Jun. 05, 2024	Update LIB and LEF.
v020	Jun. 12, 2024	Update LIB.
v021	Jul. 08, 2024	Update LIB.
v022	Oct. 09, 2024	Update datasheet.
v023	Nov. 08, 2024	Update GDS/SPI/LIB
v024	Apr. 18, 2025	Update LIB and VLG

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List of Tables

Chapter 1
Basic Information

This chapter contains the following sections:

1.1 IP Profile

Table 1.1-1 shows the IP profile.

Table 1.1-1: IP Profile

Date	2025/04/18
Product Name	TSMC CLN7FF Thermal Sensor ADC
Marketing Part No.	IGATHMX02A
Version	v024
Quality Grade (Note)	***
Top Module Name	IGATHMX02A IGATHMX02A_THMD
Technology	TSMC 7 nm 0.75 V/1.8 V CMOS LOGIC FinFET Process
Metal Scheme	IGATHMX02A: 1P7M (1X_h_1Xa_v_1Ya_h_3Y_vhv) IGATHMX02A_THMD: 1P5M (1X_h_1Xa_v_1Ya_h_1Y_v) IGATHMX02A: 1P7M (2X_hv_1Ya_h_3Y_vhv) IGATHMX02A_THMD: 1P5M (2X_hv_1Ya_h_1Y_v)
Function Description	Thermal Sensor ADC
Special Notes	N/A

Note
- * Design
- ** FPGA Verification/Simulation/Pre-silicon
- *** Silicon Proven
- ***** Mass Production

1.2 Verification Information

Table 1.2-1 shows the verification information.

Table 1.2-1: Verification Information

DRC Command File Document	T-N07-CL-DR-001-C1 1.4_1A T-N06-CL-DR-001-C1 1.1A
LVS Command File Document	T-N07-CL-LS-001-C1 1.2B T-N06-CL-SP-001-C1 1.0B
SPICE Model Document	T-N07-CL-SP-001 1.2_2P3 T-N06-CL-SP-001 1.0_2P3
Verification Condition (Note)	Silicon Report Level-3
Special Notes	N/A

Note Simulation
Silicon Report Level-1: TT with NV/NT
Silicon Report Level-2: TT with NV/NT, LV/HV & LT/HT
Silicon Report Level-3: TT, SS, and FF with NV/NT, LV/HV & LT/HT
Silicon Report Level-4: TT, SS, and FF with NV/NT, LV/HV & LT/HT, and Special Condition

1.3 Known Problems and Limitations

The following list shows the known problems and the limitations.

- DRC/ERC/ANT Error: refer to DRC/ERC/ANT Report.
- Verilog Model: for the function and the connection checks only, not for the timing check.
- Timing check: please use the timing models (LIB/DB).

1.4 DRC/ERC/ANT Violation and Waiver

Table 1.4-1: ERC Violation and Waiver

Macro Name	### ERC error ###
IGATHMX02A	floating.nxwell_float ... TOTAL Result Count = 196 (196)
IGATHMX02A_THMD	floating.nxwell_float ... TOTAL Result Count = 36 (36)

Table 1.4-2: DRC Violation and Waiver

Macro Name	### DRC error ###
IGATHMX02A	RULECHECK M1.DN.9.IP_TIGHTEN_LED ..... TOTAL Result Count = 1 (1)
	RULECHECK M2.DN.9.IP_TIGHTEN_LED ..... TOTAL Result Count = 2 (2)

Table 1.4-3: ANT Violation and Waiver

Macro Name	### ANT error ###
IGATHMX02A	N/A

1.5 Timing Model Characterization Conditions

Table 1.5-1: Timing Model Characterization Conditions

RC Corner	Process	Voltage	Temperature
typical	TT	NVDD1: 1.8 V NVDDL: 0.75 V	25 °C
rcworst_ccworst	SS	NVDD1: 1.62 V NVDDL: 0.63 V	125 °C
rcworst_ccworst	SS	NVDD1: 1.62 V NVDDL: 0.63 V	-40 °C
rcbest_cbest	FF	NVDD1: 1.98 V NVDDL: 1.045 V	125 °C
rcbest_cbest	FF	NVDD1: 1.98 V NVDDL: 1.045 V	-40 °C

Chapter 2
Version Dependency Table

This chapter contains the following sections:

2.1 Version Dependency Table

The version dependency is shown in Table 2.1-1, Table 2.1-2, and Table 2.1-3 below.

Table 2.1-1: Version Dependency Table 1

Release Note	v001	v002	v003	v004	v005	v006	v007	v008	v009	v010	v011
Datasheet	v001	v002	v003	v003	v003	v004	v005	v006	v007	v008	v008
Product Brief	v001	v001	v001	v001	v001	v001	v001	v001	v002	v003	v003
Testing Guide	N/A	N/A	N/A	N/A	N/A	N/A	v002	v002	v002	v002	v002
Verilog Model	N/A	v001	v001	v002	v002	v002	v002	v002	v003	v003	v003
Timing Model (LIB/DB)	N/A	v001	v002	v002	v003	v003	v004	v005	v005	v005	v005
LEF Model	N/A	v001	v001	v001	v001	v002	v002	v002	v002	v002	v002
DRC/LVS/ERC/ANT Report	N/A	v001	v001	v001	v001	v002	v002	v002	v002	v002	v002
Netlist (Flattened)	N/A	v001	v001	v001	v001	v002	v002	v002	v002	v002	v002
GDSII (Flattened)	N/A	v001	v001	v001	v001	v002	v002	v002	v002	v002	v002
Integration Checklist	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	v003	v003
Netlist (Phantom) (optional)	N/A	v001	v001	v001	v001	v002	v002	v002	v002	v002	v002
GDSII (Phantom) (optional)	N/A	v001	v001	v001	v001	v002	v002	v002	v002	v002	v002
IBIS Model (optional)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
CPM Model (optional)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Reference Document (optional)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 2.1-2: Version Dependency Table 2

Release Note	v012	v013	v014	v015	v016	v017	v018	v019	v020
Datasheet	v008	v009	v010	v010	v010	v011	v012	v012	v012
Product Brief	v003	v004	v005	v005	v005	v005	v005	v005	v005
Testing Guide	v002	v002	v002	v002	v002	v002	v002	v002	v002
Verilog Model	v003	v003	v003	v004	v005	v005	v005	v005	v005
Timing Model (LIB/DB)	v005	v005	v005	v005	v005	v005	v005	v006	v007
LEF Model	v002	v002	v002	v002	v002	v002	v002	v003	v003
DRC/LVS/ERC/ANT Report	v003	v003	v004	v004	v004	v004	v004	v004	v004
Netlist (Flattened)	v002	v002	v002	v002	v002	v002	v002	v002	v002
GDSII (Flattened)	v003	v003	v004	v004	v004	v004	v004	v004	v004
Integration Checklist	v003	v003	v003	v003	v003	v004	v004	v004	v004
Netlist (Phantom) (optional)	v002	v002	v002	v002	v002	v002	v002	v002	v002
GDSII (Phantom) (optional)	v003	v003	v004	v004	v004	v004	v004	v004	v004
IBIS Model (optional)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
CPM Model (optional)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Reference Document (optional)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 2.1-3: Version Dependency Table 3

Release Note	v021	v022	v023	v024
Datasheet	v012	v013	v014	v014
Product Brief	v005	v005	v005	v005
Testing Guide	v002	v002	v002	v002
Verilog Model	v005	v005	v005	v006
Timing Model (LIB/DB)	v008	v008	v009	v010
LEF Model	v003	v003	v003	v003
DRC/LVS/ERC/ANT Report	v004	v004	v005	v005
Netlist (Flattened)	v002	v002	v003	v003
GDSII (Flattened)	v004	v004	v005	v005
Integration Checklist	v004	v004	v005	v005
Netlist (Phantom) (optional)	v002	v002	v003	v003
GDSII (Phantom) (optional)	v004	v004	v005	v005
IBIS Model (optional)	N/A	N/A	N/A	N/A
CPM Model (optional)	N/A	N/A	N/A	N/A
Reference Document (optional)	N/A	N/A	N/A	N/A

Chapter 3
CAD Layer Information

This chapter contains the following sections:

3.1 Layer Information

The layer information is shown in Table 3.1-1, Table 3.1-2, Table 3.1-3, and Table 3.1-4.

Table 3.1-1: Metal Scheme of IGATHMX02A: 1P7M (1X_h_1Xa_v_1Ya_h_3Y_vhv)

Layer Name	Purpose	Layer Number	Data Type
ref	drawing	0	0
NW	drawing	3	0
OD	drawing	6	0
OD	dummy	6	7
COD_H	dummy	6	27
COD_V	dummy	6	28
COD_BLOCK	dummy	6	29
OD_18	drawing	16	0
PO	drawing	17	0
PO	dummy	17	7
CPO	drawing	17	11
CPO	dummy	17	23
VTS_N	drawing	23	0
VTS_P	drawing	24	0
PP	drawing	25	0
NP	drawing	26	0
M1	drawing	31	250
M1	odummy_a	31	252
M1	odummy_b	31	253
M1	drawing	31	255
M1	drawing	31	256
M1	dummy_a	31	258
M1	dummy_b	31	259
M2	v_high	32	230
M2	v_low	32	231
M2	drawing	32	250
M2	odummy_a	32	252
M2	odummy_b	32	253
M2	drawing	32	255

Layer Name	Purpose	Layer Number	Data Type
M2	drawing	32	256
M2	dummy_a	32	258
M2	dummy_b	32	259
M3	v_high	33	230
M3	v_low	33	231
M3	drawing	33	310
M3	odummy_a	33	312
M3	odummy_b	33	313
M3	drawing	33	315
M3	drawing	33	316
M3	dummy_a	33	318
M3	dummy_b	33	319
M4	v_high	34	230
M4	v_low	34	231
M4	drawing	34	330
M4	dummy	34	331
M4	odummy	34	337
M5	v_high	35	230
M5	v_low	35	231
M5	drawing	35	360
M5	dummy	35	361
M5	odummy	35	367
M6	drawing	36	350
M6	dummy	36	351
M6	odummy	36	357
M7	drawing	37	360
M7	dummy	37	361
M7	odummy	37	367
VIA1	drawing	51	250
VIA1	odummy_a	51	252
VIA1	odummy_b	51	253
VIA2	drawing	52	290
VIA2	odummy	52	297
VIA3	drawing	53	330
VIA3	dummy	53	331

Layer Name	Purpose	Layer Number	Data Type
VIA4	drawing	54	350
VIA4	dummy	54	351
VIA5	drawing	55	350
VIA5	dummy	55	351
VIA6	drawing	56	350
VIA6	dummy	56	351
IP	drawing	63	63
PDK	drawing	75	0
MD	drawing	84	0
MP	drawing	84	2
MD	dummy	84	7
CMD	drawing	84	20
CMD	dummy	84	27
MP	dummy	84	47
prBoundary	boundary	108	0
BJTEDMY	drawing	110	2
IBJTDMY	drawing	110	3
PSUB2	drawing	111	0
RPDMY	drawing2	115	2
RMDMY	m4	116	4
RH_TN	drawing	117	6
RH_TN	dummy	117	7
RH_TNB	drawing	117	8
text	drawing	127	0
DEXCL	m1	150	1
DEXCL	m2	150	2
DEXCL	m3	150	3
DEXCL	m4	150	4
DEXCL	m5	150	5
DEXCL	m6	150	6
DEXCL	m7	150	7
DEXCL	drawing	150	27
DEXCL	v1	150	51
DEXCL	v2	150	52
DEXCL	v3	150	53

Layer Name	Purpose	Layer Number	Data Type
DEXCL	v4	150	54
DEXCL	v5	150	55
DEXCL	v6	150	56
DEXCL	v0	150	159
DEXCL	m0	150	180
VIA0	drawing	159	250
VIA0	odummy	159	260
VD	drawing	179	250
VG	drawing	179	270
M0	drawing	180	250
M0	odummy_a	180	252
M0	odummy_b	180	253
M0	drawing	180	255
M0	drawing	180	256
M0	dummy_a	180	258
M0	dummy_b	180	259
R_rule	analog	182	3
M4	pin	202	34
M5	pin	202	35
M6	pin	202	36
M7	pin	202	37
PODE_GATE	drawing	206	28
CPODE	dummy	206	33
finBoundary	fb1	250	0
RES200	drawing	255	9
LUPDWDMY	drawing	255	59
LUPWDMY	drawinga	255	70
LUPWDMY	drawingd	255	71
LUPWDMY	drawingb	255	72
DC2	drawing1	257	21
DC2	drawing2	257	22
DC2	drawing3	257	23
DC4	drawing2	257	42
DC4	drawing3	257	43
DC5	drawing1	257	51

Layer Name	Purpose	Layer Number	Data Type
DC5	drawing2	257	52
DC6	drawing1	257	61
DC6	drawing2	257	62
DC7	drawing1	257	71
DC8	drawing1	257	81
DC8	drawing2	257	82
DC9	drawing1	257	91

Table 3.1-2: Metal Scheme of IGATHMX02A_THMD: 1P5M (1X_h_1Xa_v_1Ya_h_1Y_v)

Layer Name	Purpose	Layer Number	Data Type
NW	drawing	3	0
OD	drawing	6	0
OD	dummy	6	7
COD_H	dummy	6	27
COD_V	dummy	6	28
COD_BLOCK	dummy	6	29
OD_18	drawing	16	0
PO	drawing	17	0
PO	dummy	17	7
PP	drawing	25	0
NP	drawing	26	0
M1	drawing	31	250
M1	odummy_a	31	252
M1	odummy_b	31	253
M1	drawing	31	255
M1	drawing	31	256
M2	drawing	32	250
M2	odummy_a	32	252
M2	odummy_b	32	253
M2	drawing	32	255
M2	drawing	32	256
M3	drawing	33	310
M3	odummy_a	33	312
M3	odummy_b	33	313
M3	drawing	33	315
M3	drawing	33	316
M4	drawing	34	330
M4	odummy	34	337
M5	v_high	35	230
M5	v_low	35	231
M5	drawing	35	360
M5	dummy	35	361
M5	odummy	35	367
VIA1	drawing	51	250

Layer Name	Purpose	Layer Number	Data Type
VIA2	drawing	52	290
VIA3	drawing	53	330
VIA4	drawing	54	350
MD	drawing	84	0
MP	drawing	84	2
MD	dummy	84	7
CMD	drawing	84	20
CMD	dummy	84	27
MP	dummy	84	47
prBoundary	boundary	108	0
BJTEDMY	drawing	110	2
IBJTDMY	drawing	110	3
PSUB2	drawing	111	0
RMDMY	m4	116	4
DEXCL	m1	150	1
DEXCL	m2	150	2
DEXCL	m3	150	3
DEXCL	m4	150	4
DEXCL	m5	150	5
DEXCL	drawing	150	27
DEXCL	v1	150	51
DEXCL	v2	150	52
DEXCL	v3	150	53
DEXCL	v4	150	54
DEXCL	v0	150	159
DEXCL	m0	150	180
VIA0	drawing	159	250
VD	drawing	179	250
VG	drawing	179	270
M0	drawing	180	250
M0	odummy_a	180	252
M0	odummy_b	180	253
M0	drawing	180	255
M0	drawing	180	256
M4	pin	202	34

Layer Name	Purpose	Layer Number	Data Type
M5	pin	202	35
PODE_GATE	drawing	206	28
finBoundary	fb1	250	0
DC4	drawing3	257	43
DC6	drawing2	257	62
DC7	drawing1	257	71
DC8	drawing1	257	81
DC9	drawing1	257	91

Table 3.1-3: Metal Scheme of IGATHMX02A: 1P7M (2X_hv_1Ya_h_3Y_vhv)

Layer Name	Purpose	Layer Number	Data Type
ref	drawing	0	0
NW	drawing	3	0
OD	drawing	6	0
OD	dummy	6	7
COD_H	dummy	6	27
COD_V	dummy	6	28
COD_BLOCK	dummy	6	29
OD_18	drawing	16	0
PO	drawing	17	0
PO	dummy	17	7
CPO	drawing	17	11
CPO	dummy	17	23
VTS_N	drawing	23	0
VTS_P	drawing	24	0
PP	drawing	25	0
NP	drawing	26	0
M1	drawing	31	250
M1	odummy_a	31	252
M1	odummy_b	31	253
M1	drawing	31	255
M1	drawing	31	256
M1	dummy_a	31	258
M1	dummy_b	31	259
M2	v_high	32	230
M2	v_low	32	231
M2	drawing	32	250
M2	odummy_a	32	252
M2	odummy_b	32	253
M2	drawing	32	255
M2	drawing	32	256
M2	dummy_a	32	258
M2	dummy_b	32	259
M3	v_high	33	230
M3	v_low	33	231

Layer Name	Purpose	Layer Number	Data Type
M3	drawing	33	270
M3	odummy_a	33	272
M3	odummy_b	33	273
M3	drawing	33	275
M3	drawing	33	276
M3	dummy_a	33	278
M3	dummy_b	33	279
M4	v_high	34	230
M4	v_low	34	231
M4	drawing	34	330
M4	dummy	34	331
M4	odummy	34	337
M5	v_high	35	230
M5	v_low	35	231
M5	drawing	35	360
M5	dummy	35	361
M5	odummy	35	367
M6	drawing	36	350
M6	dummy	36	351
M6	odummy	36	357
M7	drawing	37	360
M7	dummy	37	361
M7	odummy	37	367
VIA1	drawing	51	250
VIA1	odummy_a	51	252
VIA1	odummy_b	51	253
VIA2	drawing	52	250
VIA2	odummy_a	52	252
VIA3	drawing	53	330
VIA3	dummy	53	331
VIA4	drawing	54	350
VIA4	dummy	54	351
VIA5	drawing	55	350
VIA5	dummy	55	351
VIA6	drawing	56	350

Layer Name	Purpose	Layer Number	Data Type
VIA6	dummy	56	351
IP	drawing	63	63
PDK	drawing	75	0
MD	drawing	84	0
MP	drawing	84	2
MD	dummy	84	7
CMD	drawing	84	20
CMD	dummy	84	27
MP	dummy	84	47
prBoundary	boundary	108	0
BJTEDMY	drawing	110	2
IBJTDMY	drawing	110	3
PSUB2	drawing	111	0
RPDMY	drawing2	115	2
RMDMY	m4	116	4
RH_TN	drawing	117	6
RH_TN	dummy	117	7
RH_TNB	drawing	117	8
text	drawing	127	0
DEXCL	m1	150	1
DEXCL	m2	150	2
DEXCL	m3	150	3
DEXCL	m4	150	4
DEXCL	m5	150	5
DEXCL	m6	150	6
DEXCL	m7	150	7
DEXCL	drawing	150	27
DEXCL	v1	150	51
DEXCL	v2	150	52
DEXCL	v3	150	53
DEXCL	v4	150	54
DEXCL	v5	150	55
DEXCL	v6	150	56
DEXCL	v0	150	159
DEXCL	m0	150	180

Layer Name	Purpose	Layer Number	Data Type
VIA0	drawing	159	250
VIA0	odummy	159	260
VD	drawing	179	250
VG	drawing	179	270
M0	drawing	180	250
M0	odummy_a	180	252
M0	odummy_b	180	253
M0	drawing	180	255
M0	drawing	180	256
M0	dummy_a	180	258
M0	dummy_b	180	259
R_rule	analog	182	3
M4	pin	202	34
M5	pin	202	35
M6	pin	202	36
M7	pin	202	37
PODE_GATE	drawing	206	28
CPODE	dummy	206	33
finBoundary	fb1	250	0
RES200	drawing	255	9
LUPDWDMY	drawing	255	59
LUPWDMY	drawinga	255	70
LUPWDMY	drawingd	255	71
LUPWDMY	drawingb	255	72
DC2	drawing1	257	21
DC2	drawing2	257	22
DC2	drawing3	257	23
DC4	drawing2	257	42
DC4	drawing3	257	43
DC5	drawing1	257	51
DC5	drawing2	257	52
DC6	drawing1	257	61
DC6	drawing2	257	62
DC7	drawing1	257	71
DC8	drawing1	257	81

Layer Name	Purpose	Layer Number	Data Type
DC8	drawing2	257	82
DC9	drawing1	257	91

Table 3.1-4: Metal Scheme of IGATHMX02A_THMD: 1P5M (2X_hv_1Ya_h_1Y_v)

Layer Name	Purpose	Layer Number	Data Type
NW	drawing	3	0
OD	drawing	6	0
OD	dummy	6	7
COD_H	dummy	6	27
COD_V	dummy	6	28
COD_BLOCK	dummy	6	29
OD_18	drawing	16	0
PO	drawing	17	0
PO	dummy	17	7
PP	drawing	25	0
NP	drawing	26	0
M1	drawing	31	250
M1	odummy_a	31	252
M1	odummy_b	31	253
M1	drawing	31	255
M1	drawing	31	256
M2	drawing	32	250
M2	odummy_a	32	252
M2	odummy_b	32	253
M2	drawing	32	255
M2	drawing	32	256
M3	drawing	33	270
M3	odummy_a	33	272
M3	odummy_b	33	273
M3	drawing	33	275
M3	drawing	33	276
M4	drawing	34	330
M4	odummy	34	337
M5	v_high	35	230
M5	v_low	35	231
M5	drawing	35	360
M5	dummy	35	361
M5	odummy	35	367
VIA1	drawing	51	250

Layer Name	Purpose	Layer Number	Data Type
VIA2	drawing	52	250
VIA3	drawing	53	330
VIA4	drawing	54	350
MD	drawing	84	0
MP	drawing	84	2
MD	dummy	84	7
CMD	drawing	84	20
CMD	dummy	84	27
MP	dummy	84	47
prBoundary	boundary	108	0
BJTEDMY	drawing	110	2
IBJTDMY	drawing	110	3
PSUB2	drawing	111	0
RMDMY	m4	116	4
DEXCL	m1	150	1
DEXCL	m2	150	2
DEXCL	m3	150	3
DEXCL	m4	150	4
DEXCL	m5	150	5
DEXCL	drawing	150	27
DEXCL	v1	150	51
DEXCL	v2	150	52
DEXCL	v3	150	53
DEXCL	v4	150	54
DEXCL	v0	150	159
DEXCL	m0	150	180
VIA0	drawing	159	250
VD	drawing	179	250
VG	drawing	179	270
M0	drawing	180	250
M0	odummy_a	180	252
M0	odummy_b	180	253
M0	drawing	180	255
M0	drawing	180	256
M4	pin	202	34

Layer Name	Purpose	Layer Number	Data Type
M5	pin	202	35
PODE_GATE	drawing	206	28
finBoundary	fb1	250	0
DC4	drawing3	257	43
DC6	drawing2	257	62
DC7	drawing1	257	71
DC8	drawing1	257	81
DC9	drawing1	257	91

Chapter 4
Errata

IGATHMX02A does not have any errata at this stage.