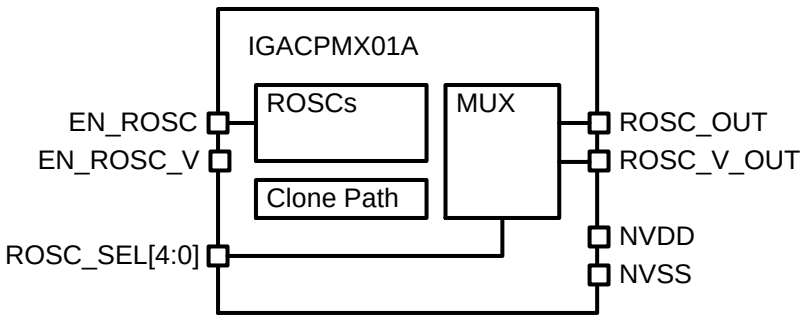
IGACPMX01A

TSMC CLN7FF

Chip Performance Monitor

Overview

IGACPMX01A is an on-chip performance monitor which contains a maximum of 32 customized multiple ring oscillators. This macro is one sensor unit of chip performance and process monitor system. The controller, IGDOMC002A, will control this macro to read out the frequency of ring oscillators. The SoC system can use this frequency of different ring oscillators to come out with one formula to be the reference for chip performance or critical path timing, and the control system can be implemented to perform Adaptive Voltage Scaling (AVS) and Dynamic Voltage and Frequency Scaling (DVFS) of SoC chip. Besides the customized ring oscillator, the macro also supports one clone path of chip performance for monitoring correlation checks.



Functional Block Diagram

Features

- Supports one clone critical path ring oscillator customization
- Maximum 32 internal ring oscillators
- Supply voltage range: -20 % to +50 %, from 0.6 V to 1.125 V (Typ. 0.75 V)
- Target > 95 % timing correlation
- Supports disable mode
- Operating junction temperature: -40 °C ~ 125 °C
- Macro size: 45 µm (width) x 100 µm (height)

Technology

- Process: TSMC 7 nm 0.75 V/1.8 V CMOS LOGIC FinFET Process
- Special layer & device:
  - Core device:
    SVT, LVT, and ULVT
  - Resistor: Metal R resistor
- Metal scheme:
  1P7M
  (1X_h_1Xa_v_1Ya_h_3Y_vhv)
  1P7M (2X_hv_1Ya_h_3Y_vhv)

Applications

- AVS
- DVFS
- Process monitor
- Chip binning

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Testing Guide	.pdf
5	Verilog Model	.v
6	Timing Model	.lib/.db
7	LEF Model	.lef
8	DRC/LVS/ERC/ANT Report	.rep
9	Netlist (Flattened)	.spi
10	GDSII (Flattened)	.gds
11	Integration Checklist	.xlsx
12	Netlist (Phantom) (optional)	.spi
13	GDSII (Phantom) (optional)	.gds
14	IBIS Model (optional)	.ibs
15	Reference Document (optional)	.pdf

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GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC IP Eco-System provides the flexibility to work with IP from GUC, TSMC, and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

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