CH4

Innovation and Green R&D

Annual Targets and Performance

Integrating sustainability thinking into innovation and R&D is a critical driver for responding to the rapid transformation of the semiconductor industry. As an upstream industry participant, GUC provides advanced custom IC design services based on customer requirements, delivering the cells, functions, and code required for chip design through silicon intellectual property (IP), while embedding green design principles into the development of high-performance, low-power, and reusable products. Operating under a fabless model that does not involve chip manufacturing or factory operations, the Company continues to pursue the dual objectives of resource efficiency and environmental compatibility through sustained R&D investment and quality management.

United Nations Sustainable Development Goals (SDGs)

Corresponding Material Topics

R&D and Innovation　　Product Quality & Safety

Item	2025 Annual Target	2025 Annual Performance	Achieved
Patent Applications	>10	>10	✓
R&D Expenditure	>NT$3 billion	NT$ 3.3 billion	✓
Low-Power, High-Performance Products	Continuous development	Continuous development	✓
Sustainable Product Revenue Ratio	>70%	88%	✓
ISO Quality Management System Certification	Maintained	ISO 9001 — Green Products QC 080000 Medical Products ISO 13485 Quality System Certification	✓
Product Regulatory Compliance and Hazardous Substance Management	Material regulatory penalties: 0 incidents Customer complaints / returns due to hazardous substances: 0 incidents	Material regulatory penalties: 0 incidents Customer complaints / returns due to hazardous substances: 0 incidents	✓
Customer Service Satisfaction	>90%	95%	✓

4.1 Professional IC Design Services and Innovative Technologies

GUC provides professional IC design services, with a particular focus on the design of Application-Specific Integrated Circuit (ASIC) products. To meet the requirements of products from concept to finish product with Advanced ASIC Services, GUC collaborates with TSMC to advance high-performance, low-power technologies such as CoWoS, InFO, and 3DIC. The Company also incorporates IP solutions and leverages artificial intelligence in Electronic Design Automation (EDA) to optimize design processes. By partnering with academia, GUC further advances AI technology applications in design services, boosting its market competitiveness. GUC offers optimized solutions for product realization through the following three service models and capabilities:

Custom Design Services (Non-Recurring Engineering, NRE)

Provides circuit design component libraries and various silicon intellectual properties needed for product design, as well as circuit diagrams for manufacturing product mask sets. The Company then commissions foundries to produce masks, wafers, dicing, and packaging, after which the Company's engineers conduct product testing before delivering prototypes to customers.

Multi-Project Wafer Program (MPW)

Provides a cost-effective and timely chip verification service by integrating designs from different customers, sharing the manufacturing costs of a single mask set and one batch of wafers (Engineer Run). This allows design engineers to achieve low cost and rapid prototype verification using advanced process technology before mass production.

Silicon Intellectual Property (IP)

Designed and verified integrated circuit designs with specific functions that can be reused. With advancements in integrated circuit manufacturing technology, multi-function chips and even SoC have become the mainstream in IC design. Reusable IP can reduce customers' duplicate design efforts and design resource investments.

4.1.1 Providing Advanced ASIC Services

The semiconductor industry supply chain can be divided into four major groups according to upstream, midstream, and downstream: design, manufacturing, packaging, and testing. For the upstream chip design group, the chip design flow goes beyond hardware specification design and also requires software design support. Only after high automation integration can highly efficient, low-power consumption chips be designed at extremely tiny nanometer dimensions. GUC offers upstream IC design services to meet rapidly changing semiconductor industry and diverse customer demands. Our Advanced ASIC Services framework allows customers to enter the semiconductor design industry chain at any stage, from product concept, specification formulation, development, verification, final completion.

Specifically, GUC provides advanced special IC design services through the following four core capabilities:

IP Solution	Chip Implementation	ASIC Manufacturing	Advanced Packaging Technology
Help customers reduce design time costs and minimize SoC development risks to meet their customized requirements.	The Company works closely with TSMC, giving a strong command of information on advanced manufacturing processes. This expertise allows us to help customers accelerate their entry into advanced process, achieve faster mass production, improve yield rates, and strengthen market competitiveness.	In addition, GUC actively partners with world-class wafer foundries, packaging and testing companies, and other supporting suppliers to deliver professional, high-quality manufacturing services. This collaboration shortens time-to-market and time-to-volume, lower entry barriers and technical risks, and ensures high quality, high yield rates, and on-time delivery. As a result, customers can focus their valuable resources on their core strengths.	GUC deploys advanced process design platform solutions and advanced packaging technologies, working with TSMC to complete the design and verification of CoWoS, InFO, and 3DIC, meeting the requirements for high performance, low latency, and low power consumption. GUC also continues to develop IPs such as HBM, GLink, and UCIe needed for advanced packaging platforms.

4.1.2 Artificial Intelligence (AI) Technology Applied to IP Design and Design Services

In recent years, the rapid development of Artificial Intelligence (AI) has become an indispensable technological tool for enterprise research and development. When used properly, it can enhance efficiency and reduce waste of resources. GUC IP design team has prioritized the implementation of AI technology for the Monte Carlo simulation, saving computational resources and enabling a 50% reduction in simulation time. This allows limited resources to be reallocated to more design projects. In addition, GUC has completed the evaluation of AI-based design migration solutions, which help design engineers optimize circuits for enhanced results and reduce the design cycle by 30%. Formally implemented in Q2 2025.

GUC introduced Engineering Change Orders (ECO) tools in 2020, reducing leakage optimization time by 15-30%. In 2023, AI automatic placement and routing technologies and tools were implemented, saving 2-8% in power efficiency. In 2024, we continued collaborating with leading electronic design automation (EDA) vendors to introduce AI-driven EDA technologies for automated floorplan optimization. Preliminary results demonstrated area reductions of approximately 3% alongside improvements in power efficiency. In addition to leveraging AI for design optimization, the Company completed an evaluation of AI knowledge base assistants combining EDA vendor tools with large language models (LLMs) in Q4 2025, and procured the corresponding AI GPU servers. Deployment to engineering staff is scheduled to commence in Q2 2026 to enhance and support engineers' training and knowledge development in EDA. In addition to adopting AI-driven technologies from EDA companies, GUC collaborates annually with academia to develop AI and machine learning applications for 2D/3D EDA design flows. These academic partnerships aim to integrate advanced technologies into GUC design service processes, enhancing design quality, efficiency and optimization, and applying the innovations to customer products.

4.1.3 Functional Safety Implementation Technology Applied to Automotive Design Services

GUC has introduced functional safety (FuSa) implementation technologies and established corresponding design implementation service workflows, encompassing: (1) system-level logic and memory built-in self-test (BIST) enabling vehicles to autonomously verify critical components; (2) implementation workflows compliant with USF or SSF function safety format-aware methodologies; and (3) incorporation of functional safety considerations into design-for-test (DFT) techniques for critical signals. These approaches enable implementations featuring dual-core or triple-register-redundancy decision logic and physical verification to achieve reduced failure rates. These technologies enhance the safety of customers' automotive products and were successfully applied in two customer projects in 2025. We will continue to monitor developments and advance new technologies to make future automotive products safer and more reliable.

4.2 Innovative R&D and Quality Management

In 2025, GUC continued to invest in innovation and R&D, with full-year R&D expenditure reaching NT$3.3 billion, reinforcing technical capabilities and enhancing product quality in support of long-term sustainable development.

The CoWoS and InFO chiplet architectures employed by the Company have become mainstream infrastructure product platforms. Leveraging close collaboration with key partners, GUC's R&D team has accumulated extensive multi-year experience in the development of High Bandwidth Memory (HBM), GUC multi-die interLink (GLink), and Universal Chiplet Interconnect Express (UCIe) IP, as well as in the high-volume manufacturing of CoWoS products. To support customers in achieving competitive advantage in advanced 2.5D/3D packaging and sustaining their market leadership positions, GUC continues to demonstrate its long-term commitment to delivering the most competitive end-to-end 2.5D/3D solutions — encompassing the aforementioned IP, electrical and thermal simulation, package design, DFT and production test, and CoWoS and InFO manufacturing expertise.

4.2.1 Successful Technology Development and Innovation Achievements in 2025

GUC was honored at the 2025 EE Awards Asia with the Best EDA & IP/Processor — 5th Anniversary Award

In addition to the ongoing development of silicon IP for advanced process nodes (5/4/3/2 nm and beyond) — including UCIe, GLink-2.5D/3D, HBM2/2E/3/3E/4/4E Controller and PHY, and high-speed ADC/DAC — existing foundational IP components such as Power Management Solutions and Clock Generators are also being continuously ported to more advanced process nodes to provide customers with a more comprehensive solution portfolio. GUC was honored at the 2025 EE Awards Asia with the Best EDA & IP/Processor — 5th Anniversary Award, in recognition of the Company's technical excellence and quality capabilities in silicon IP design.

To position for future growth, the Company continues to allocate R&D resources toward optimizing 5/4/3/2 nm design flows and advancing the development of GUCIe, GLink, GLink 3D, HBM PHY & Controller, and high-speed ADC IP.

2025 Innovation Achievements Summary

IP Development

Most Recent Program	Current Status
3 nm HBM4E 12G Controller and PHY IP Development	Test chip design finalized
5 nm UCIe LP 32G IP Development	
5 nm UCIe LP 32G Face-Up IP Development	
3 nm UCIe 64G IP	
3 nm And 5 nm Custom GLink-3D IP Development	
16 nm IVR Technology Development	

Design Flow

First Quarter
- Function safety aware USF/SSF design flow completed

Second Quarter
- N2P v1.0 design flow completed
- First customer automotive project using USF design flow completed — design finalized and taped out in Q2 2025
- Completed N3P/N5 GLink-3D customer project

Third Quarter
- Second customer automotive project using USF design flow completed — design finalized and taped out in Q3 2025

Fourth Quarter
- 3Dblox 3.0 Advanced Packaging Design Flow completed

4.2.2 Green Product Quality and Competitiveness

In a competitive market environment, the Company encourages employees to uphold a spirit of innovation and continuous improvement, delivering high-quality design services, silicon IP, and competitive products to customers, while building credible and mutually beneficial long-term partnerships through attentiveness to customer needs. Through a PDCA-based quality management mechanism, the Company ensures the effective operation of its quality management system, continuously improves operational performance, and advances toward its goal of becoming a globally leading IP and ASIC provider.

In the area of ASIC IC design services, the Quality and Reliability organization continues to strengthen its quality management system, maintaining annual ISO 9001 management system certification, systematically reviewing and improving quality management processes to ensure customer satisfaction and enhance overall quality performance.

In the area of green product management, green design principles are embedded from the product design stage. Through continuous technological innovation, the Company addresses customers' stringent hazardous substance management requirements and progressively reduces and regulates the use of prohibited substances. In accordance with International Electrotechnical Commission (IEC) standards, the Company maintains its IECQ QC 080000 Hazardous Substance Process Management system certification and completed recertification through third-party body DQS in 2025, with the updated certificate valid through August 2028.

In addition, green IC products comply with the EU RoHS Directive and REACH Regulation, ensuring the absence of prohibited substances. In response to customer requirements, the Company completed multiple conformance surveys in 2025, encompassing IPC 1752, chemSHERPA material declarations, and U.S. TSCA regulations, with results provided to customers for reference. Quarterly business reviews (QBRs) are also conducted with key suppliers, incorporating hazardous substance conformance assessment items and regularly reviewing implementation outcomes to ensure that production processes comply with regulatory and customer requirements.

In addition, we have been recognized by leading international customers for our green product management efforts. We are a certified Sony Green Partner and, in 2025, received the Green Product Certificate from key customer SK hynix and the Eco-Partner certification from Samsung. These recognitions demonstrate our customers' strong confidence in GUC's green product management capabilities.

GUC QualityManagement System Certifications Overview

- GUC ISO9001 Certification

- GUC IECQ QC080000 Certification

- Sony Green Partner certification

- GUC ISO 13485 Medical Certification

- SK hynix Green Partner Certification

- GUC Samsung "Eco-Partner" Certification

Strengthening Quality Culture

To deepen quality culture and internalize quality thinking into day-to-day operations, the Company encourages employees to proactively propose improvement initiatives, continuously refining quality management practices to address customer requirements and enhance overall competitiveness. Through the annual Best Known Method (BKM) competition, the Company reinforces problem-solving capabilities and systematizes and standardizes best practices, continuously building capacity in quality management and technical innovation.

BKM proposal outcomes over the years have been successfully converted into key technical patents — with 2 patents granted and 3 applications filed — demonstrating the substantive impact of quality improvement activities on R&D innovation and technology accumulation. The following are representative cases of quality and efficiency improvement:

BKM Case 1

HBM4 Power-Aware Signal Integrity Design with Crosstalk Cancellation on CoWoS-R 8RDL to Achieve 12Gbps

To address the growing demands of AI and HPC, our team utilized the CoWoS-R platform to develop a 12 Gbps HBM4 interface. This BKM achieved three key breakthroughs in Signal and Power Integrity design: crosstalk cancellation design, decoupling path optimization for advanced package, and advanced packaging layer count reduction. The details are as follows:

1. **Crosstalk Cancellation Design:** By optimizing the signal routing topology on the CoWoS-R advanced package, this breakthrough achieves over 25% crosstalk cancellation in worst-case scenarios. This significantly enhances signal quality for the 12Gbps HBM4 interface and improves energy efficiency.
2. **Decoupling Path Optimization for Advanced Package:** To address Power Integrity challenges, this BKM optimizes the placement of Integrated Passive Devices (IPD) and power plane connectivity within the CoWoS-R advanced package. This design effectively reduces the decoupling path inductance by 39.34%. Furthermore, by integrating DCIR analysis results, this BKM established comprehensive design guidelines for IPD placement, thereby enhancing the stability of the Power Delivery Network (PDN).
3. **Advanced Packaging Layer Count Reduction:** Through electromagnetic (EM) field analysis, we optimized the Return Path and bump re-pitch architecture. Even under high routing density conditions, our team successfully reduced the advanced packaging layer count by 10% while maintaining excellent eye diagram quality. This optimization directly decreases material consumption during the manufacturing process.

Furthermore, to address the extremely complex electrical requirements of HBM4, this BKM integrates the above breakthroughs into a standardized Advanced Packaging-Level Hard Macro, located directly beneath the IP Block. By standardizing complex SI/PI optimization design, future designs only need to manage signal interconnects to achieve compliance. This BKM significantly shortens the development cycle, effectively reduces design risks and trial production failure rates, which transforms technical know-how into long-term corporate R&D assets..

BKM Case 2

Failure Reduction Methods for ACScan Production Vmin

Growing customer demand for high gate-count and high-power projects has made IR drop and production Vmin loss as key factors to manage. To address this, we propose a BKM with three key strategic to minimize Vmin loss:

1. **Low-IR DFT design**
2. **Flow & Pattern optimization**
3. **Wafer process optimization**

Implement a robust low-IR DFT architecture, including flexible design for Scan-mode separation and MBIST serial. Maintain adequate bump/solder count for VDD/VSS. CDA(Clock Delay Adjustment) optimization. Apply backup IR reduction circuits and ensure sufficient toggle rate margin. Optimize clock gating, clock shift waveform and data gating ◦ Utilize worst-case CPM for IR/ATE hardware PI simulation. Tighten ATE hardware PI spec.

This BKM significantly improved production Vmin loss to sub-percentage failure rate, enlarge Vmin production window and reduce potential RMA and stable shipment quantity.

BKM Case 3

AI Project Efficiency Enhancement Methodology

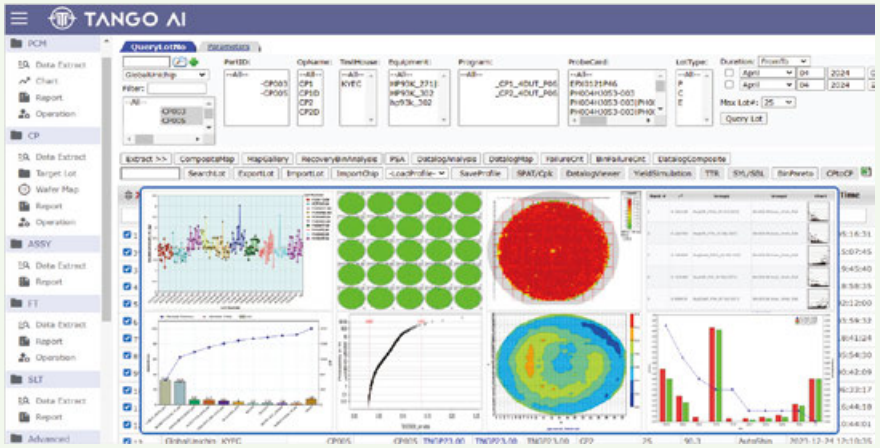
To improve overall efficiency in large-scale AI chip design projects, multiple design flow and tooling optimization measures were proposed to effectively address design bottlenecks and enhance quality and resource utilization efficiency, including:

1. **NOC Design:** Physical Synthesis and Timing Closure Strategy
2. **Fishbone Clock Tree Structure for Hold Time Protection:** Another significant improvement involves the traditional clock tree structure, which tends to result in excessive clock cells and wasted resources. The fishbone clock tree structure provides an optimized solution, particularly for hold time protection. This structure reduces the need for delay cells, improving clock efficiency. The optimized clock tree reduces delays per channel and has been applied across multiple channels, resulting in substantial efficiency gains and reducing resource consumption.
3. **A Mechanism to Improve Front-End Engineer (FE) Efficiency:** Regarding front-end engineering (FE) efficiency, a major challenge has been the manual handling of large amounts of data, particularly when clients release data. A semi-automated utility tool has been developed to assist FE engineers. This tool automates the data check-in process, allowing engineers to automatically fill in parameters for all flow. This utility greatly enhances overall productivity and the efficiency of FE engineers.
4. **Design-Aware DFT (Design for Test) Plan:** For the DFT (Design for Test) process, traditional tools struggle to manage the complexity of large AI chip designs. The new approach introduces DFT partitioning based on data flow, eliminating the need for wrapper implementations. This method simplifies the DFT insertion process, reducing the time required for testing and verification.

These changes have collectively addressed key bottlenecks in the design process, improving both efficiency and performance in AI chip design and environmental impact.

Enhancing Product Quality

GUC employs the Tango system to monitor real-time production WAT/test data. We continuously optimize our product quality control mechanisms and improves product yield to ensure quality and safety.



4.2.3 Customer Service and Satisfaction

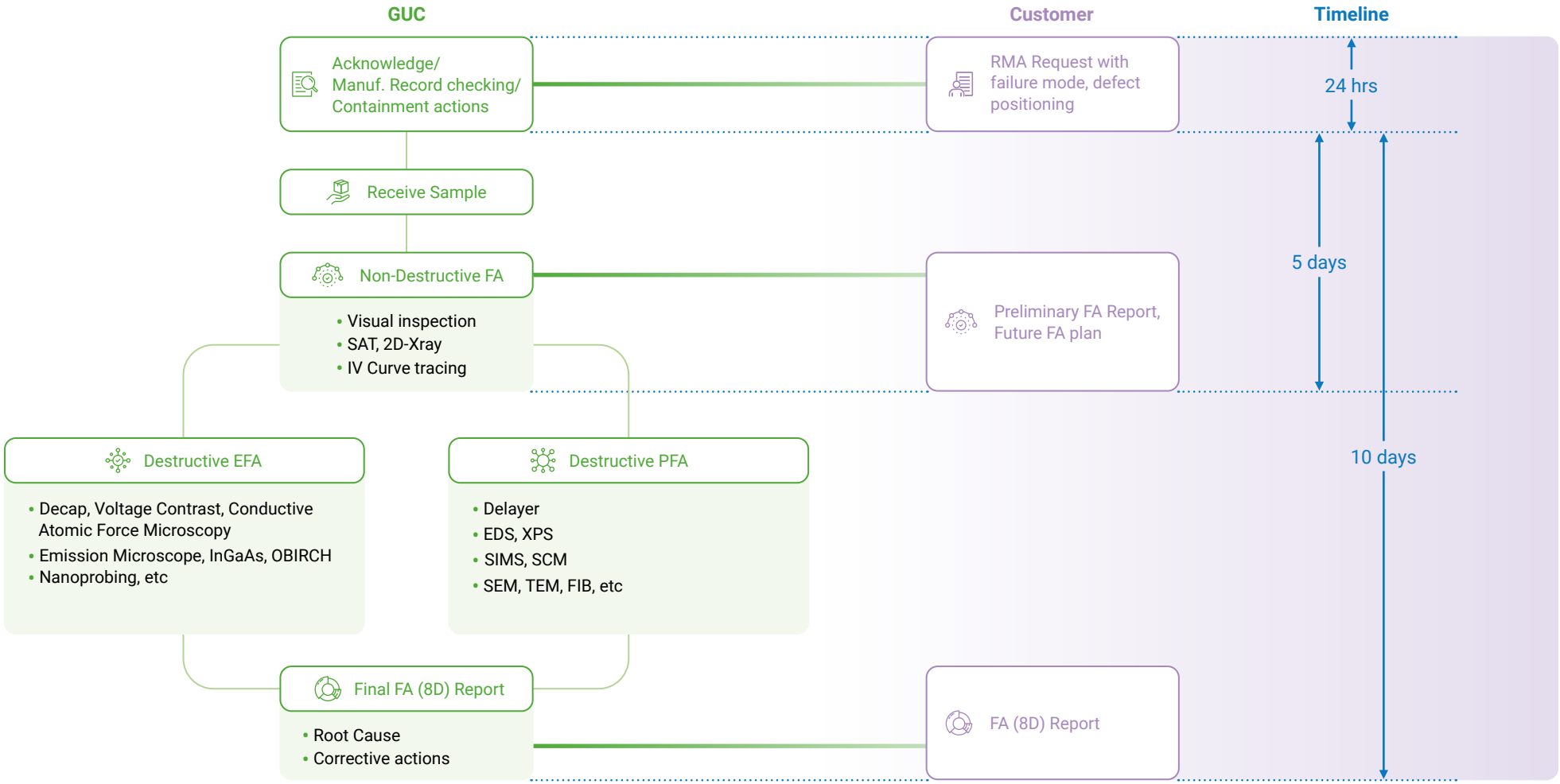
In addition to maintaining management system certifications, GUC ensures the delivery of high quality IC design services. We also strengthen customer relationship management through regular and irregular meetings and visits, as well as quarterly and monthly performance reviews or audits. These efforts help build seamless partnerships and align both parties with short, medium, and long-term development goals and social responsibility initiatives. To provide localized customer service, we have established dedicated offices in six regions—Taiwan (headquarters), China, Japan, Korea, the United States, and Europe—with dedicated service contacts. These contacts support the planning and implementation of environmental management, social responsibility, hazardous substance control, and conflict minerals between both parties, while complying with ISO9001 and accepting third-party verification. We promptly provide sufficient information to meet the needs of downstream and end customers, or public sectors, and actively cooperate with customers' corporate social responsibility programs to implement activities, investigations, audits, and data collection.

To ensure customer satisfaction with GUC's service quality, we conduct customer satisfaction surveys annually in the first quarter or upon project completion. Customers are invited to provide feedback on GUC's service quality and effectiveness through ratings, comments, or comparisons with competitors. A dedicated customer satisfaction team follows up with concrete responses, tracks improvement progress across responsible departments, and performs detailed data analysis to identify root issues. These results are compiled into reports for senior management as reference for medium and long-term operational planning.

Customer satisfaction surveys over the past five years have consistently achieved a response rate of over 80%, with more than 90% of respondents rating their satisfaction with GUC as "Satisfied" or higher. This reflects GUC's ability to continuously enhance service effectiveness and maintain high customer satisfaction amid technological advancements and a highly competitive business environment. In the 2025 customer satisfaction survey, the majority of customers provided highly favorable assessments, citing attributes including professional and reliable design capabilities and services, rapid response capability, a stable supply chain framework, and consistent production quality assurance.

Customer Satisfaction Survey Summary

To manage customer complaints, we have established a Customer Complaint Management Procedure requiring the relevant departments to respond to customers within 24 hours of complaint receipt and to provide a preliminary analysis report within 5 business days. In 2025, the on-time response rate for preliminary analysis reports reached 90%. No product recalls attributable to quality or safety concerns occurred during the year.

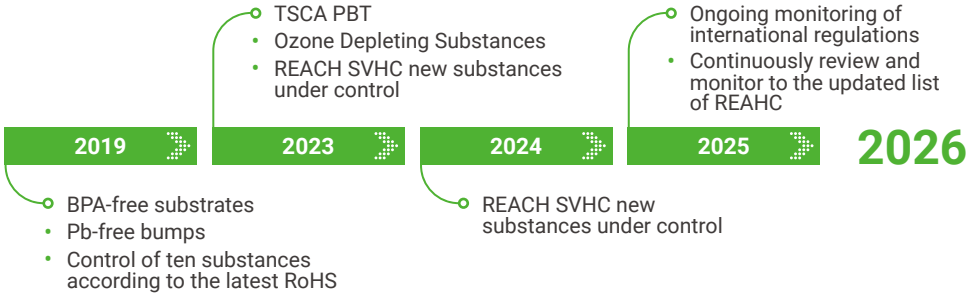


4.2.4 Green Product Sustainable Management and Practices

GUC implements a PDCA management process for green product sustainable management to address regulatory risks. Improvement strategies are proposed through supplier surveys, and we work closely with the supply chain to prevent the use of hazardous substances. These efforts aim to proactively respond to international regulatory trends and enhance the competitiveness of GUC products. To ensure that green IC production processes comply with regulatory requirements, quarterly business reviews (QBRs) are conducted with key suppliers, with implementation outcomes evaluated on a quarterly basis. In 2025, all GUC products met customer and regulatory requirements without any compliance violations, and all design materials adhere to the special requirements for customers' green products.

Our objective is to ensure that 100% of shipped products conform to customer and regulatory requirements, as well as customers' specific green product requirements.

Product Hazardous Substance Control Program



ACT

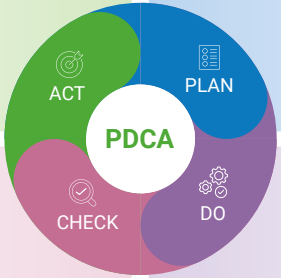
- Raw material hazardous substance test
- Suppliers are required to provide the proof of compliance with hazardous substance test report issued by ISO 17025 certified labs

- Require suppliers to provide third-party test reports to ensure the compliance of raw material and meet with GUC specification.

PLAN

- Regulatory identification and customer requirements
- Restricted substance regulations
- Planning for hazardous substance substitution

- The European Union has added 9 new substances to the Registration, Evaluation, Authorization and Restriction of Chemicals (REACH) regulation. In 2025, the EU candidate list has been expanded to 251 SVHCs. GUC complied with all new requirements. We continuously monitor updates to the REACH regulations and have obtained supplier compliance declarations that are 100% compliant with the new requirements.
- Identifying the use of per- and polyfluoroalkyl substances (PFAS) throughout the supply chain and continuously monitoring regulatory developments.



CHECK

- Management Review: The top management review the achievement of hazardous substance KPIs.
- Customer Satisfaction: Annual customer satisfaction surveys regarding green product management are conducted to review customer feedback.

- Achieve 89% customer satisfaction rating high ratings and positive recognition for green product sustainable management. We are recognized by customer SK hynix to obtain Green Partner Certification in Feb'25

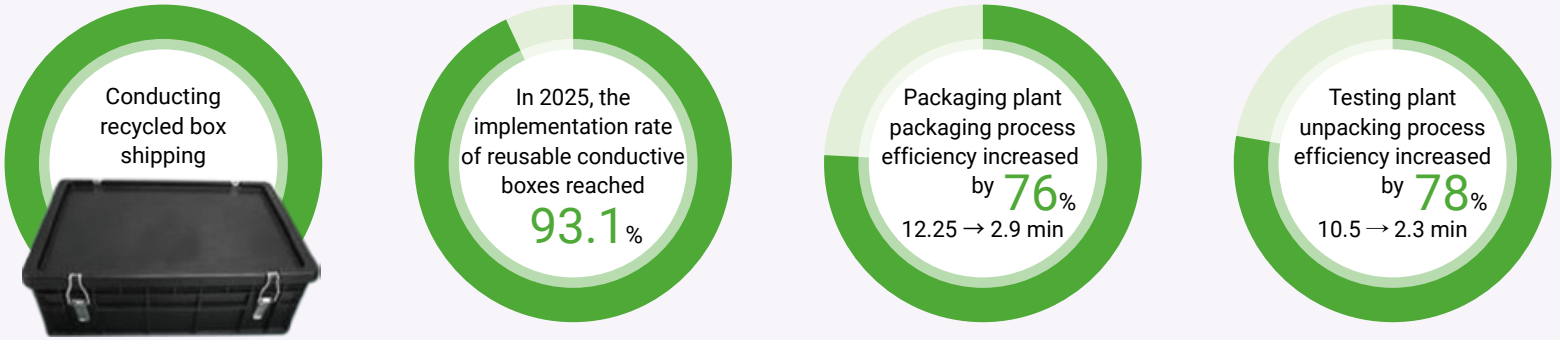
DO

- Evaluate and Review Material from product Eco-Design Stage
- Implement elimination of Hazardous substance program

- In the Bill of Materials (BOM) material selection phase, 11 new product BOMs were added in 2025, adopting green IC specifications. In response to the strengthening of PFAS regulations globally, and given that the relevant proposal is currently in the final evaluation stage at ECHA, Perfluorinated and polyfluorinated alkyl substances (PFAS) are known as 'forever chemicals' as they are extremely persistent in our environment and bodies. They can lead to health problems such as liver damage, thyroid disease, obesity, fertility issues and cancer. PFAS are of concern because of their high persistence (or that of their degradation products) and the impacts on human and environmental health. GUC is committed to proactively reducing hazardous substances from the product design stage, continuously monitoring applicable regulations and environmental risks, and conducting advance assessments. Upon any EU prohibition announcement, the Company will achieve compliance immediately. GUC continues to evaluate PFAS usage and requires suppliers to monitor fluorine (F) content. The Company will also continue working with suppliers to review and assess all potentially hazardous substances that may impact the environment and human health, with a view to adopting safer alternative materials.

4.2.5 Hazardous Substance Sustainable Management and Actions Throughout Product Life Cycle

Measures	Green IC Design and Requirements	Green Material Selection	Green IC Manufacturing	Green Packaging Use
Description	GUC responds to customer requirements for green materials by adhering to green procurement procedures and selecting materials that comply with international regulations, including RoHS, EU chemical policy (REACH), with the EU candidate list increased to 251 substances in 2025, and continues to monitor updates to the REACH regulated substance list. As well as Ozone Depleting Substances (ODS), and Persistent, Bioaccumulative and Toxic (PBT) substances under the US TSCA. To ensure environmental protection, all products use halogenfree materials, and we actively seek alternative materials to avoid the use of harmful substances in raw materials.	In the Bill of Materials (BOM) material selection stage, GUC actively conducts risk assessments, with 11 new product BOMs added in 2025, adopting green IC specifications. At the same time, GUC sets strict restrictions on product materials to eliminate harmful substances, aiming to prevent any part of the production processes from potentially impacting the environment, such as contributing to global warming and ozone layer depletion.	GUC has strengthened its hazardous substance management mechanism by requiring suppliers to monitor hazardous substances in raw materials and to provide third-party test reports to ensure compliance with green product principles and international regulations. In 2025, all customer-commissioned investigations were able to provide customers with compliance investigation results.	Product packaging materials are restricted according to the Packaging Directive (94/62/EC). The following are GUC's concrete actions to comply with international regulations and promote circular economy: • Green IC production requirements for restricting hazardous substances in product packaging: In 2023, the France Decree 2020-105 was added, which regulates mineral oil substances in ink packaging. Mineral oil saturated hydrocarbons (MOSH) and mineral oil aromatic hydrocarbons (MOAH) have been proven to be carcinogenic and bioaccumulative. To comply with international regulatory trends and safeguard customer health, 100% supplier conformance has been achieved. • Introduction of reusable conductive boxes: Considering the environmental impact of discarded packaging materials, GUC has adopted reusable conductive boxes to replace single-use cardboard boxes, implementing waste reduction, recycling conductive boxes back to the factory for reuse, and recycling, aiming to minimize environmental impact. Additionally, GUC has simplified the packaging process for products transported from the packaging plant to the testing plant. This includes streamlining packaging and unpacking processes, such as eliminating inner packaging steps for large boxes, which also reduces operational time waste. In 2025, the implementation rate of reusable conductive boxes reached 93.1%.



As a significant participant in the global electronics supply chain, GUC is committed to environmentally friendly eco-design (Eco-Design) in electronic products. With respect to the widespread use of bisphenol A (BPA) in electronic components, we are committed to systematically reducing and ultimately eliminating BPA from its products. Beginning in 2019, all new products have fully adopted 100% BPA-free substrate key components to reduce long-term environmental impact and advance sustainable corporate development.

Lead (Pb), a hazardous substance commonly encountered in electronics manufacturing processes, is both a reproductive toxicant and a carcinogen that poses risks to human health. The Company tracks regulatory developments under the EU RoHS Directive (Restriction of Hazardous Substances). In relation to the lead exemption applicable to passive components, a comprehensive audit of passive components across all products was conducted. The audit findings confirmed that all passive components used in the Company's products are lead-free (Pb-free). EU RoHS Exemption 7(c)-I is not utilized, and all products are fully compliant with RoHS requirements. The transition to lead-free production has been completed.

4.3 Patents and Silicon Intellectual Property

GUC is committed to developing a broad range of competitive silicon IP, including High Bandwidth Memory IP, die interconnect IP, mixed-signal front-end IP, and SoC IP. To safeguard the outcomes of innovative research and development, GUC files patent applications for competitive technical solutions generated throughout the ASIC design and production service stages. In parallel, we implement patent strategies for our proprietary Silicon Intellectual Property (IP). By securing patent protection, GUC not only maximizes the benefits and competitive edge of its R&D achievements but also offers customers enhanced protection for their ASIC products. Since its establishment, GUC has obtained 610 patents from various countries. In recent years, the company has been actively deploying patents related to CoWoS, HBM, UCIe, G-Link, and other technologies to maintain its leading position and competitive advantage.

Recognizing the importance of patent rights, GUC has been offering colleagues with intellectual property-related in-person courses annually since 2016. These courses aim to strengthen awareness of patent rights and promote momentum for patent proposals.

Number of Granted Patents by Country

Country	Number of Patents
Taiwan	235
United States	225
China	132
Japan	18

Intellectual Property Rights Management

GUC established the Intellectual Property Management Regulations in 2016. Since 2000, the Company has been promoting intellectual property rights management plans and has formulated the Patent Proposal Application Procedure as a guideline for patent application, maintenance, utilization, and bonuses/rewards related matters. To carefully evaluate patent proposals, the Company has further established an internal patent review mechanism called the Patent Committee. Committee members include senior executives from relevant departments and heavyweight professors specially appointed from the IC design field externally. Through the committee's internal review and opinions, the technical content of invention proposals can be made more complete, effectively ensuring patent quality and increasing the probability of patent approval. In the past three years, the Company has filed a total of 71 patent applications in various countries, with 49 cases completing the examination process. Among these, 49 were granted and 0 were abandoned, while the rest are still under examination. This demonstrates that our company's patent allowance rate across various countries is as high as 100%. In addition, for patent proposals that are unsuitable for public disclosure but have technical value, the Patent Committee may decide to protect them as trade secrets instead, preventing the leakage of confidential technologies.

In addition, to effectively enhance management efficiency, GUC introduced the Patent Management Information System in 2015 as an information management platform for patent proposals, applications, maintenance, bonus distribution, technology classification, and product applications. With the support of this information system, GUC enhances the protection of confidential patent information, while also improving staff efficiency and reducing human errors in the patent application processes.

Additionally, GUC regularly conducts patent inventory operations to review the application status of patents and their degree of relevance to related products, providing an evaluation of patent value. To further strengthen awareness and respect for patent rights among R&D personnel, and to prevent violations of patent boundaries, the Company requires all new R&D personnel to complete basic patent courses. In addition to foundational patent coursework, the Company regularly invites guest lecturers from the patent industry to provide R&D personnel with practical intellectual property training, covering advanced topics including patent search, infringement analysis, and design-around strategies. As of 2025, cumulative course attendance has reached 245 participants.

To maintain a leading position in industry technology, GUC adopts a strategy that integrates key operational development objectives with intellectual property rights protection. For specially developed Silicon Intellectual Property (IP) and Advanced Packaging Technology (APT)—such as CoWoS, HBM, UCIe, and G-Link—patent engineers collaborate with relevant R&D personnel to review the research, development, design processes, and outcomes to evaluate the feasibility of patent applications. For projects with patent layout potential, GUC actively files patent applications and continuously tracks the proposal progress. By progressively implementing patent layout for specifically developed Silicon Intellectual Property (IP), GUC not only strengthens its competitive edge in specific fields but also implements the Silicon Intellectual Property (IP) Project/IC Product Patentization to fulfill the goal of securing patent protection for key Silicon Intellectual Property and IC product developments. Meanwhile, the Company conducts regular patent technology inventories as a basis for managing the correlation between patent intellectual property and Silicon Intellectual Property (IP), as well as for evaluating the value of patent intellectual property.

To ensure that senior management fully understands the implementation of our intellectual property management plan, the legal supervisor reports on relevant matters to the Board of Directors at least once a year. The legal supervisor completed the annual report on October 30, 2025.

4.4 Green Product Design Services

Sustainable Product Revenue

As a global leader in IC design services, GUC is committed to delivering high-performance, low-power ASIC design services that help customers reduce energy consumption and carbon emissions across artificial intelligence, high-performance computing, networking, and smart applications. We define our sustainable product scope to encompass proprietary IP and design technologies that deliver power efficiency improvements (high performance, low power), as well as products that generate green carbon reduction benefits at the customer level. This scope reflects the Company's ongoing commitment to advancing the energy transition and environmental responsibility within the semiconductor industry.

Over the past three years, GUC's sustainable product revenue has grown continuously. In 2025, sustainable product revenue reached NT$30 billion, representing 88% of total revenue. Through the continued development of low-power design technologies and green IP, GUC enhances product value while supporting global customers in achieving their energy efficiency and carbon reduction objectives. GUC maintains an extensive IP portfolio and advanced design platform, driving sustainable value through innovative technologies while strictly adhering to international standards including RoHS, REACH, and conflict minerals requirements.

Going forward, we will continue to leverage its innovation, R&D, and green design capabilities to support customers in building more sustainable systems and applications, advancing the semiconductor industry's low-carbon transition together.

	2023	2024	2025
Sustainable Product Revenue (NT$/ NTD)	17,649,704,830	18,208,688,940	30,086,790,348
Sustainable Product Revenue Ratio	67%	73%	88%
Annual Target – Sustainable Product Revenue Ratio		70%	

Low-Power Chip Design and Energy Efficiency Management

Silicon Intellectual Property (IP)	**High Bandwidth Memory IP (HBM4 IP)** GUC's latest-generation 3nm 12G High Bandwidth Memory (HBM4) completed Tape out in Q1 2025. Power design optimization is currently underway; through low-power design techniques, energy consumption is targeted for a 50% improvement, with IP revision expected to be completed in Q2 2026.
	Universal Chiplet Interconnect Express IP (UCIe) In early 2022, GUC released UCIe 1.0, a die-to-die interface specification aimed at unifying standard and advanced packaging formats and enabling ecosystem collaboration for multi-die integration. GUC continues to leverage its GLink-2.5D experience and expertise in the development of next-generation GUCIe. Compared to the existing 3nm UCIe PHY design, the 5nm UCIe was developed to a low-power specification targeting a 15% reduction in energy consumption. Test chips was ready in Q4 2025 and entered the testing phase; actual measurement data are expected to be obtained by Q2 2026. The UCIe 32G IP was recognized as the Best IP of the Year at the 2024 EE Awards Asia, a testament to GUC's technological capabilities and development excellence.

Silicon Intellectual Property (IP)	**Die-Stacking Interface IP (GLink-3D)** 3D packaging is an advanced technology that increases transistor density. As an industry leader, GUC has partnered with TSMC to develop the GLink-3D 1.0 product, enabling 3D SoIC stacking for 5nm and 6nm chips. The validation report was completed in 2024. The next-generation GLink-3D 2.0 delivers further specification enhancements, enabling die stacking between 5nm and 3nm chips. By adopting a finer bond pitch, signal bandwidth density is improved by approximately three times while power consumption is reduced by 80%. The forthcoming GLink-3D 3.0 is scheduled to complete design by mid-2026, enabling die stacking between 3nm and 2nm chips, with continued focus on increasing signal bandwidth density and reducing power consumption.
System-on-Chip (SoC)	**System-on-Chip / Silicon Intellectual Property Automatic Integration Process (SoC / IP Constructor, unicoRn)** Since 2021, GUC has successfully completed a range of chip designs, including 16nm autonomous driving chips (Automotive), 12nm 5G networking chips (Networking). In 2022, the team completed 7nm virtual reality chips (Metaverse). In 2023, the department completed 5nm data center-grade AI chips (Datacenter AI) and production version of 16nm automotive chips. In 2024, the SOC department finalized 5nm edge AI chips and the advanced version of 16nm virtual reality chips. In 2025, GUC completed mass production of a 5nm data-center-grade AI chip and testing of an advanced 16nm virtual reality chip. • Over the years, GUC has relied on: 1. Enhanced R&D capacity and industry-leading integration verification processes, effectively reducing pre-processing time by 30~50%. 2. Early identification of critical debugging items during integration, saving 30~50% of resources that would otherwise be used for extensive functional simulation and late-stage regression debugging. 3. Optimization of chip specifications based on manufacturing process advancements, improving performance by 20~30%, reducing power consumption by 15~20%, and decreasing chip area by 20~30%. • The System-on-Chip / Silicon Intellectual Property automatic integration process is as follows: STEP 1 Critical subsystem (processor, high-speed interface, memory) integration platform (Subsystem) STEP 2 Hardware accelerator-based advanced verification process (Emulation) STEP 3 Low-power design verification and optimization (Power profiling) STEP 4 Software and hardware co-verification process (Virtual / Hybrid platform)
Design Service	GUC completed its first N2 test chip tapeout in 2024 and finalized testing and verification along with the N2P v1.0 design flow in Q2 2025. This enables customers to rapidly adopt more advanced, high-efficiency process nodes. Through improvements in EDA software and design flows under equivalent design verification conditions, the overall design flow achieves optimized power consumption and performance. Compared to N3E, N2P v1.0 delivers further power reduction, achieving 25% power savings. We will continue developing N2P and future A16 nanometer design flows to support IP designs with lower power manufacturing processes, enhance competitiveness, apply them to customer projects, and accelerate customers' progress toward greener products.