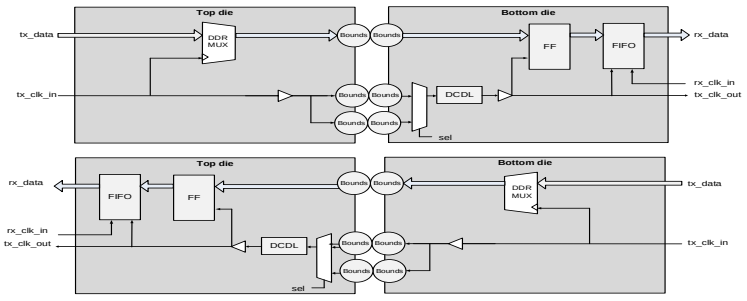
ZGAD2DA05A

TSMC CLN2P GLink-3D DDR Die-to-Die PHY

Overview

ZGAD2DA05A is a GLink-3D high-speed Die-to-Die interface PHY IP. ZGAD2DA05A includes both the TX PHY IP and the RX PHY IP. ZGAD2DA05A enables data transmission between dies using TSMC System on Integrated Chips (SoIC-X) 3D stacking technology (3DFabric), supporting Chip-on-wafer (CoW) assembly with face-to-face die stacking. Communication is established through the TX IP on the top or bottom die, transmitting data to the RX IP on the corresponding die. An embedded RX CDC FIFO ensures reliable data handling. The TX and RX IPs adopt a symmetrical physical layout floorplan for hybrid bond (HB) mapping. ZGAD2DA05A provides several configurations based on a basic 600-bit TX PHY IP and a basic 600-bit RX PHY IP. The data lanes transfer at bit rates ranging from 1.0 Gbps at 0.550 V to 3.8 Gbps at 0.675 V, with all operating conditions maintained within this range.

Each IP contains PMAD and PMAA modules. PMAA supports double data rate (DDR) transmission on data bits. PMAD provides parity generation, checker, and lane repair functions. PMAD also provides full Scan support, Loopback, BIST generator, and checker.



ZGAD2DA05A Block Diagram

Features

- Supports SoIC-X (3DFabric) CoW assembly
- Supports face-to-face die stacking
- Supports point-to-point communication between single TX and single RX
- Data rate per bond: from 1.0 Gbps at 0.550 V to 3.8 Gbps at 0.675 V
- TX/RX lanes transfer in DDR manner
- Implemented several configurations based on a 600b basic unit with 300 data lanes
- Include 4 lanes for parity generation and checking in each 600b unit for TX and RX respectively
- Include 8 lanes for data lanes repair and 1 lane for clock lane repair in each 600b unit for TX and RX respectively
- 0.037 pJ/bit power consumption considering level shifter, bus split, and bus re-assembly
- Supports near-end loopback mode, Scan, and BIST
- Support DVFS
- Single logic core power domain supply
- The IP can be configured by APB, I^2C, or JTAG interfaces

Technology

- Process:
  TSMC 2nm 0.75V CMOS LOGIC NanoSheet Plus Process
- Special Layer & Device: SoIC-X related layers
- Metal Scheme:

  TD:
  1P19M_1X1XB1XC1XD1YA1YB6Y2YY2YX2R_UHP3MIM_UT-sRDL
  BD:
  1P19M_1X1XB1XC1XD1YA1YB6Y2YY2YX2R_UHP3MIM_UT-sRDL_sTSV

Deliverables

Item	Description	Format
1	Release Note	.pdf
2	Datasheet	.pdf
3	Product Brief	.pdf
4	Verilog Model	.v
5	Timing Model	.lib/.db
6	LEF Model	.lef
7	DRC/LVS/ERC/ANT/CNOD Report	.rep
8	Netlist (Flattened)	.spi
9	GDSII (Flattened)	.gds
10	ROM Model (Reduced Order Model)	binary database
11	Emulation Model	.v

About Global Unichip Corp. (GUC) Design Excellence

GUC, the Advanced ASIC Leader, provides a comprehensive suite of Advanced ASIC Services from silicon-proven IP to complete SoC integration and delivery. Founded in 1998, GUC is publicly traded on the Taiwan Stock Exchange. GUC design services cover all fabrication technologies from mature processes up to the most advanced technology node. At the most advanced nodes, high complexity, noise coupling, electromigration, dynamic IR drop, and design for manufacturing (DFM) problems now exceed the capability of traditional design methodology. That's why GUC provides an advanced technology design flow that includes a quick prototyping step to achieve rapid timing and signal integrity closure.

As an added assurance, all GUC IP are silicon-proven and designed with manufacturability, test, and yield considerations in mind. GUC provides a total IP solution through FPGA platform verification for a variety of products.

GUC IP Eco-System provides the flexibility to work with IP from GUC, TSMC, and other vendors, creating the widest range of design options. Based in Hsinchu Taiwan, GUC has developed a global reputation with a presence in China, Europe, Japan, Korea, and North America. With a solid track record of shipping more than 150 million complex SoC units to date, GUC provides the fastest time-to-market at the lowest possible risk.

For more information about this product or other GUC services please visit us on the web at www.guc-asic.com