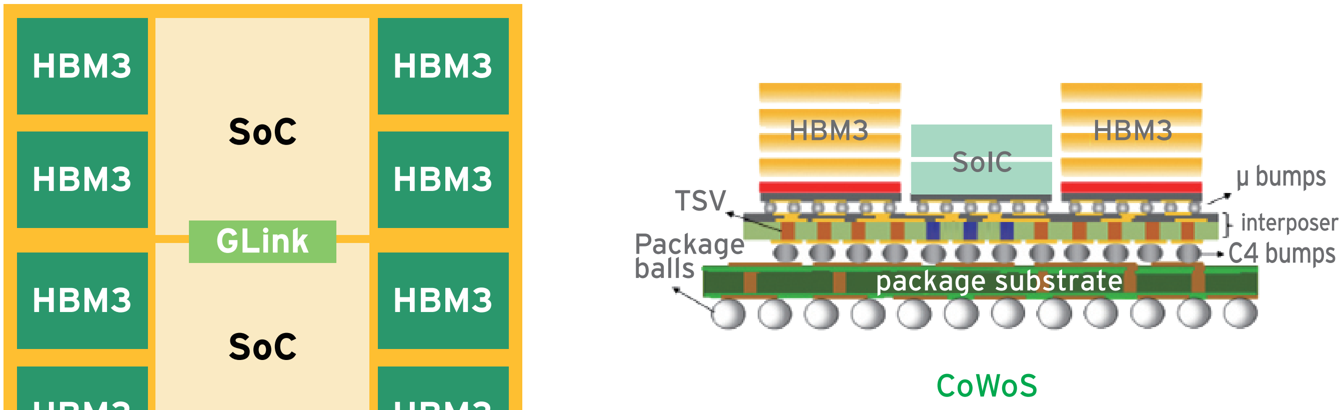
2022Q3

Leadership in AI & HPC Turnkey Total Solution

The Advanced ASIC Leader

APT Total Solution

- Technology leadership in APT (Advanced Packaging Technology)
- High performance 16nm / 12nm / 7nm / 6nm / 5nm / 3nm ASIC solution for AI & HPC applications
- Comprehensive integration of 4 ~ 8 HBM2E/ 3 memories and high-lane-count SerDes using CoWoS with system-level power, signal, and thermal integrity solution
- Chiplet system solution with GUC multi-die interlink (GLink) for low-latency applications
- Experiences in 400~700 mm^2 16nm / 12nm / 7nm / 5nm ASIC die with 300W~700W power consumption
- Fully synchronous operation of thousands of processing elements at 2+ GHz
- Unit-level DFT redundancy for high yield with big chip
- SI (Signal Integrity), PI (Power Integrity), and thermal co-simulation of 2.5D / 3D / InFO package design with complex subsystem integrations

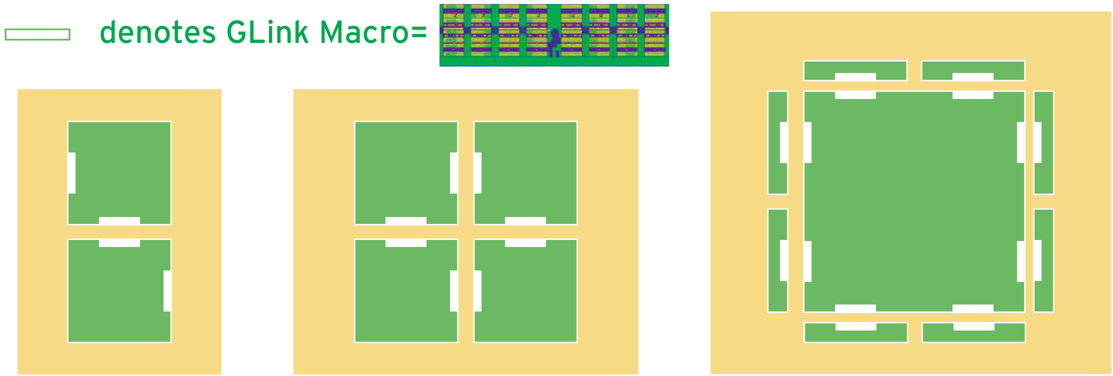


CoWoS

Example using HBM with CoWoS

GUC multi-die interLink (GLink) Solution Tailored for AI & HPC

- Competitive power, performance, and form factor for multi-die integration with InFO_oS / CoWoS advanced packaging technologies
- Optimized for AI / ML, Super Computing, Networking ASIC designs



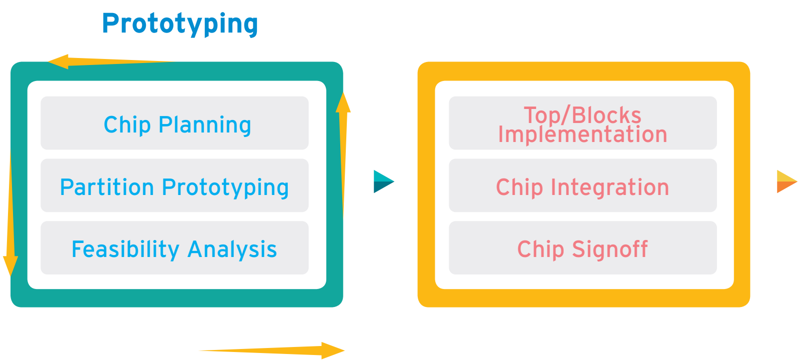
Dual-Die Package

Quad-Die Package

Chiplet & Main SoC

Experienced Large Scale Design

- 5B+ gate count design
- 200+ lanes of high-speed SerDes integration
- Repeated-block aware service



Prototyping

- Chip Planning
- Partition Prototyping
- Feasibility Analysis

- Top/Blocks Implementation
- Chip Integration
- Chip Signoff

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