

GUC 2.5D and 3D multi-die APT Platform

GUC
The Advanced ASIC Leader

GUC provides Industry-leading 2.5D and 3D multi-die advanced packaging technology (APT) platform for AI, HPC and Networking ASICs.

Platform Highlights

Silicon Proven HBM3 and CoWoS Technology

- HBM3 Controller and PHY, running at 4.8 - 8.4 Gbps
- TSMC CoWoS-S and CoWoS-R technology

Industry-Leading Die-to-Die Interface IP (GLink-2.5D)

- Highest bandwidth: 2.5 Tbps/mm (full duplex)
- Lowest power: 0.30 pJ/bit

Cutting-Edge Die-on-Die Interface IP (GLink-3D)

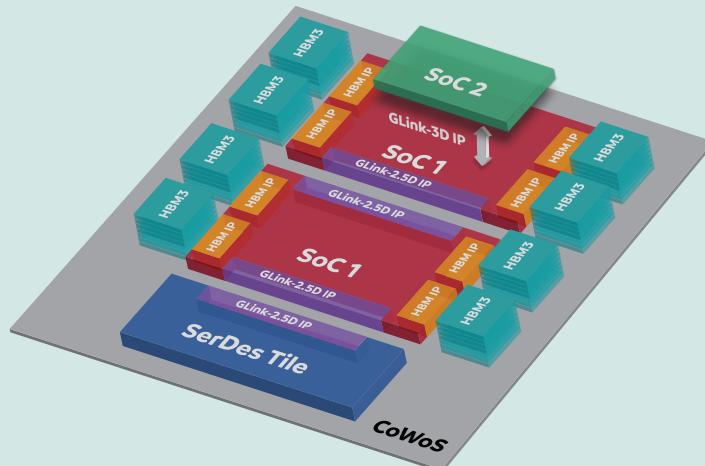
- As high as 9 Tbps/mm² (full duplex)
- TSMC SolC CoW (Chip-on-Wafer) and WoW (Wafer-on-Wafer) technology

Platform Highlights

- HBM3 PHY + Controller IP
- Die-to-die IP (GLink-2.5D)
- Die-on-die IP (GLink-3D)
- High speed IP integration
(112G SerDes, PCIe-5, GDDR6)
- Advanced Packaging Technology
(CoWoS / InFO / 3D-SoIC)

Service Scope

- SoC and ASIC design to production
- Interposer and RDL design
- SI/PI/IR/THM simulation
- Package and substrate design



Service Scope

Service	2.5D (Die-to-Die)	3D (Die-on-Die)
Flagship SoC Design	<ul style="list-style-type: none"> Advanced Process : N3E/N4P/N5/N6/N7 SoC design from customer spec-in to GDS SoC Integration with Key IP : HBM, GLink, 112G SerDes, PCIe5, GDDR6 Hundred lanes of 112G SerDes SI, PI, and IR Analysis 	
GUC IP Solution	<ul style="list-style-type: none"> HBM2E/3 PHY & Controller GLink-2.5D 1.0/2.0/2.3(LL) Lane/bump repair methodology IP customization & IP sub-system built 	<ul style="list-style-type: none"> GLink-3D 1.0/2.0(LL) Optimized TSV utilization & bond map Lane/bond repair methodology IP customization & IP sub-system built
TSMC 3DFabric™ Technology	<ul style="list-style-type: none"> CoWoS-S (Silicon Interposer) CoWoS-R (RDL Interposer) InFO_oS (Integrated Fan-Out) 	
2.5D/3D Design	<ul style="list-style-type: none"> GUC patented Interposer & RDL design 2.5D DFT methodology 	<ul style="list-style-type: none"> Multi-die timing closure DTC design and integration 3D DFT methodology
Package Design	<ul style="list-style-type: none"> Substrate design 2.5D/3D multi-die SI, PI and Thermal Cosim & Analysis of ring and lid packages 	
Production	<ul style="list-style-type: none"> Qualification, characterization, 2.5D and 3D manufacturing management, tight yield control, high volume production 	

GUC HEADQUARTERS, HSINCHU, TAIWAN
+886-3-564-6600
oliver.shyu@guc-asic.com

GUC TAIPEI
+886-2-8797-5658
kevin.chen@guc-asic.com

GUC NORTH AMERICA
+1-408-382-8900
jerryc.chen@guc-asic.com

GUC CHINA
+86-21-3366-5868
brad.chou@guc-asic.com

GUC JAPAN
+81-45-222-8256
alex.huang@guc-asic.com

GUC KOREA
+82-10-3352-0083
jeff.lin@guc-asic.com

GUC EUROPE B.V.
+31-6-4412-9373
christelle.faucon@guc-asic.com