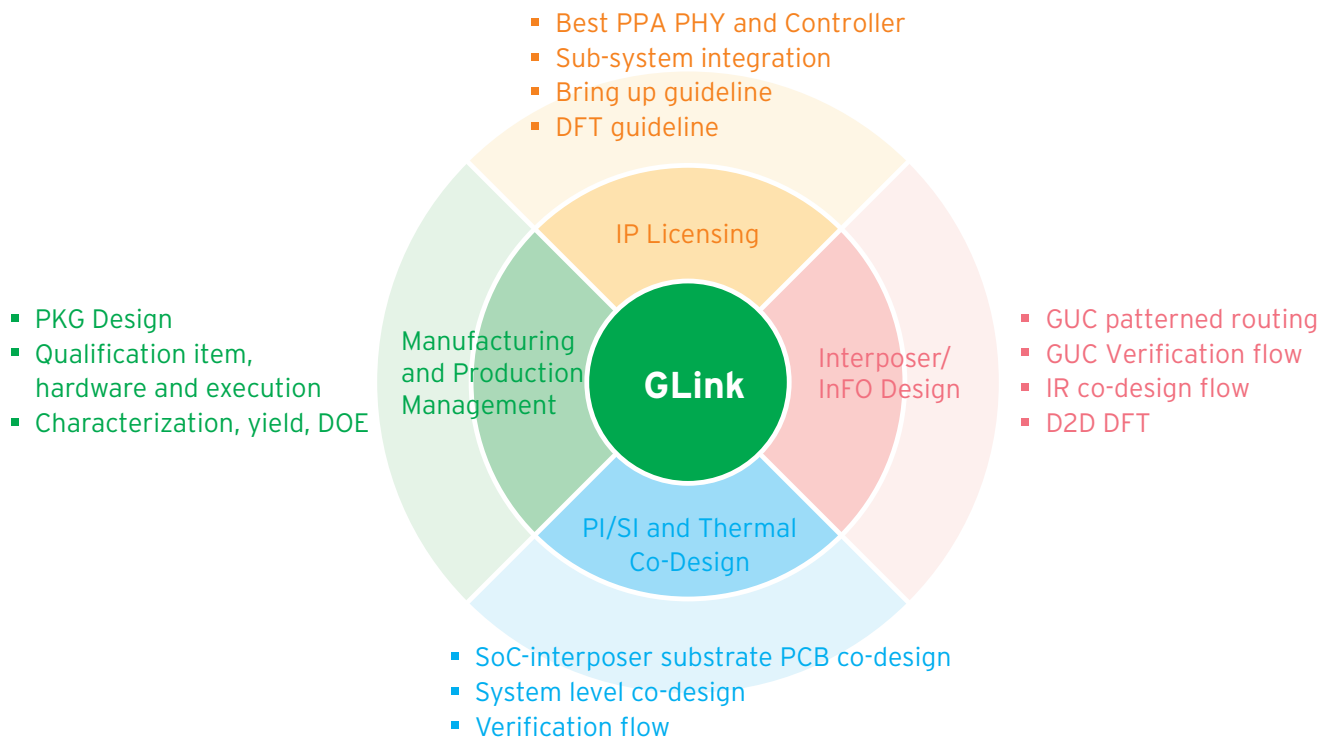
GUC multi-die interLink(GLink) IP

Overview

GUC multi-die interLink (GLink) IP provides world's best class solution for high-bandwidth, low-power, low-latency multi-channel interconnection in a package for applications such as High Performance Computing, Data Center, Artificial Intelligence and Networking.

The IP utilizes single-ended DDR clock forwarding parallel bus interface with TSMC's RDL-based InFO (Integrated-Fan-Out) or CoWoS (Chip-on-Wafer-on-Substrate) up to 8/16 Gbps per lane which consumes only around 0.3pJ/bit. One slice of GLink 1.0/2.0 has 32 full-duplex lanes and one PHY of GLink 1.0/2.0 has 8 slices with 2/4Tbps maximum bandwidth. For the next generation GLink, one slice will have 56 full-duplex lanes and one PHY has 8 slices with 7.6 Tbps maximum bandwidth.

Based on the great success of GLink die-to-die IP family, GUC continues to develop the standard-compliant UCIe IP with enhanced features. The first N5 UCIe-compliant IP will be taped out in 1H23 to serve the performance and robustness demand of large chip and chiplet interconnect.



GLink Key Features

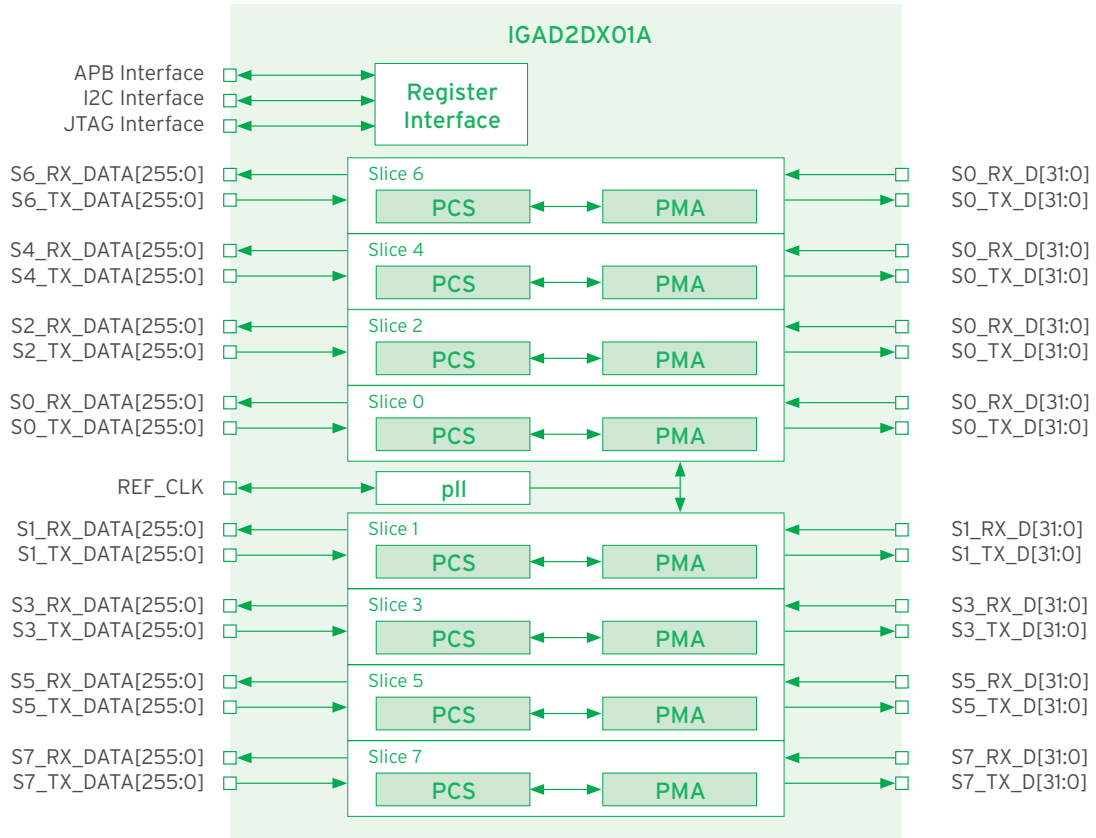
GLink 1.0/2.0

- 0.25pJ/bit (1.0) and 0.3 pJ/bit (2.0) power consumption
- Up to 8Gbps per lane (1.0) and 16Gbps (2.0) per lane
- 2 Tbps/3mm (1.0) and 4 Tbps/3mm (2.0) beachfront (TX and RX)
- 32 full-duplex lanes per slice
- 8 slices are included in one hard macro
- Lane repair
- Data Bus Inversion
- Parity bits for error detection
- Built-in test pattern generator and checker
- Independent power down mode for analog blocks
- Operating junction temperature: -40°C ~ +125°C

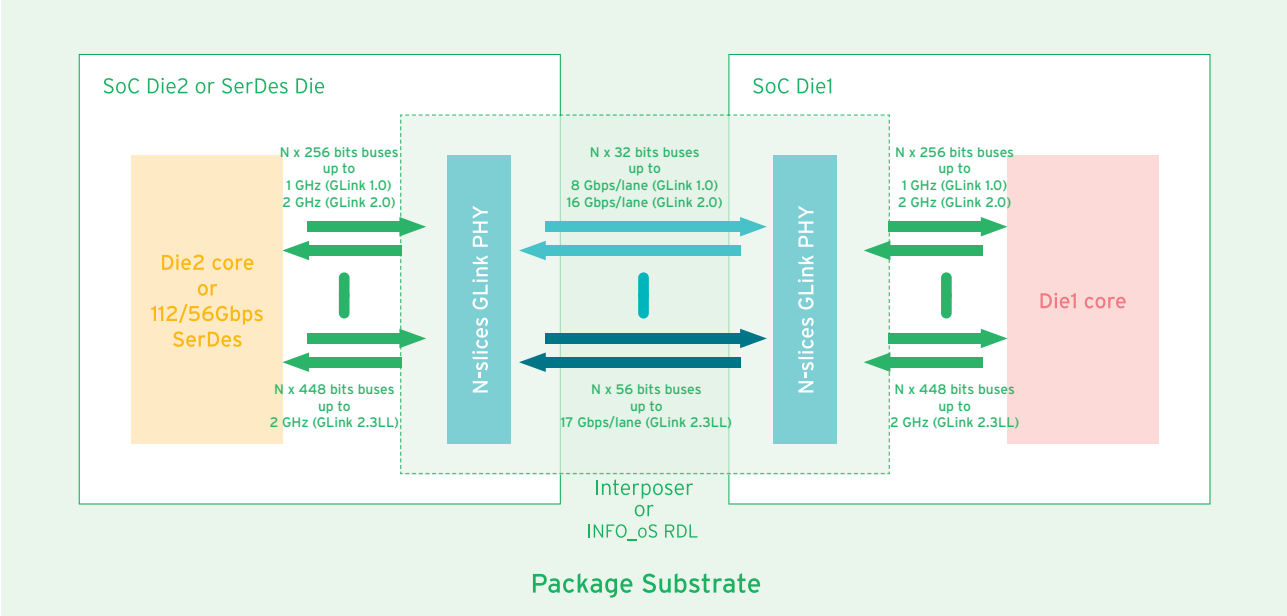
GLink 2.3LL

- 0.3pJ/bit power consumption
- Up to 17Gbps per lane
- 7.6 Tbps/3mm beachfront (TX and RX)
- 56 full-duplex lanes per slice
- 8 slices are included in one hard macro
- Low Latency
- Lane repair
- Data Bus Inversion
- Parity bits & CRC for error detection
- Built-in test pattern generator and checker
- Independent power down mode for analog blocks
- Operating junction temperature: -40°C ~ +125°C

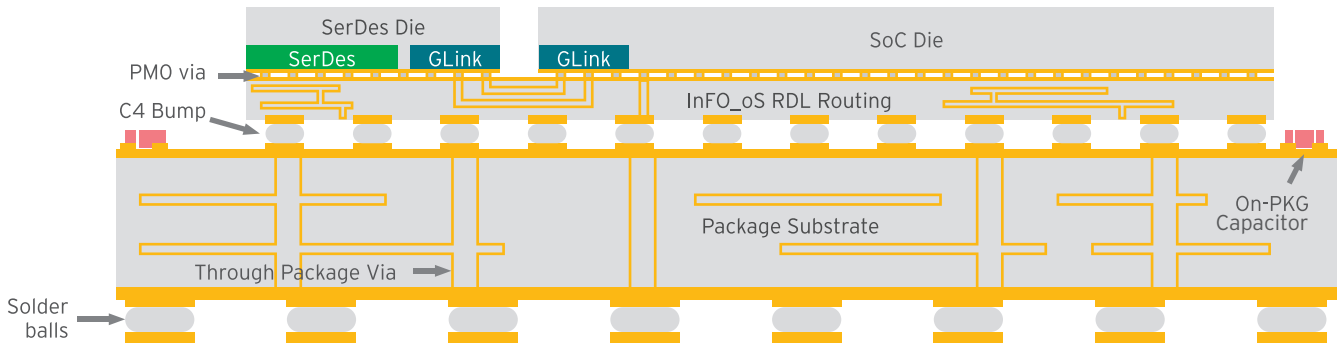
Block Diagram



Integration Examples



2.5D InFO Package Side View



GUC multi-die interLink (GLink) IP Portfolio

● Production ● Pilot

IP NAME	FEATURE	BEACHFRONT	PROCESS	STATUS	IP CODE
GLink 1.0	8Gbps/lane	2Tbps/3mm	N7 N6	●	IGAD2DX01A
GLink 2.0	16Gbps/lane	4Tbps/3mm	N5	●	IGAD2DY01A
GLink 2.3LL	17Gbps/lane	7.6Tbps/3mm	N5	●	IGAD2DY04A
GLink 2.3LL	17Gbps/lane	7.6Tbps/3mm	N3E	Design Kit: 2023/Q1	IGAD2DZ01A

GUC

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